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Research paper

Low-component design and behavioral modeling of a 343-level inverter system

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ABSTRACT

In this study, design and performance aspects of a 343-level asymmetrical cascaded inverter system specially designed for renewable energy systems are presented. The proposed inverter is operated and analyzed under three distinct configurations. The system is designed using unequal DC voltage sources with the structure (1:2:7:14:49:98)Vdc, producing a 343-level output. In the first case, Vdc is set to 1 V (per-unit system), while in the second case it is set to 40 V, resulting in actual voltages of (40:80:280:560:1960)V with a total maximum of 3920 V. In the third case the Vdc sources are replaced with photovoltaic (PV) modules. The simulations reveal that the inverter provides improved performance in producing low-distortion voltage and current waveforms closely approximating a sine wave. With the per-unit voltage case and power factor of 0.92, the inverter realizes an RMS voltage (Vo_{RMS}) and current (Io_{RMS}) of 120.9316 V and 3.7178A, and total harmonic distortion of voltage (THD_{Vo}) and current (THD_{Io}) of 0.32422% and 0.22506%, respectively. While with actual voltage values and power factor of 0.97, the results set Vo_{RMS} of 4838.7577 V and Io_{RMS} of 6.7445A with THD_{Vo} of 0.32414% and THD_{Io} of 0.25682%. For the PV module configuration with a power factor of 0.92, the inverter records Vo_{RMS} of 4827.9768 V and Io_{RMS} of 148.4073A with THD_{Vo} of 0.90328% and THD_{Io} of 0.54142%. These results show the flexibility of the inverter to deliver an enhanced power output with low harmonic distortion and the suggested inverter has significant potential for use in modern renewable energy systems and industrial applications.

1. Introduction

The incorporation of renewable energy supply into the existing power system has increasingly become important in the last few years mainly because of increasing energy needs and global warming effects. Among the various technologies developed for high-efficiency energy conversion, MLIs have shown strong potential for improving the impact of photovoltaic (PV) systems in grid integration. A few research articles discuss and present the potential of MLI topologies for the combination of solar PV systems with the grid. A comprehensive survey of MLI topologies describing successful implementation of MLI for solar PV grid integration to enhance efficiency and reduce harmonics was presented [1]. This paper presents a novel 343-level asymmetrical cascaded inverter that, to the best of the authors' knowledge, achieves the highest level count (343) with the minimum switch count (18) reported in literature for single-phase configurations. Unlike existing high-level MLI designs that require 20+ switches for similar or lower level counts, the proposed topology utilizes an optimized asymmetric voltage ratio (1:2:7:14:49:98) combined with PDLSPWM control to maximize output resolution while minimizing component requirements. The specific contributions of this work include: (1) a novel switch configuration enabling 19.06 levels per switch—the highest ratio reported for >100 level inverters; (2) seamless integration with photovoltaic sources using modular boost-MPPT interfaces; and (3) comprehensive validation under dynamic environmental conditions including variable irradiance and temperature, demonstrating practical applicability in real-world

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renewable energy systems. A new multilevel inverter configuration is presented in this paper to achieve higher efficiency, low cost and better performance in renewable energy systems. Based on the simulation and experiment, the design is a major improvement in the power conversion for sustainable energy systems [2]. Some authors proposed a new innovative integrated multilevel inverter configuration aimed at tackling renewable energy transformation problems focusing on the power quality enhancement and scalability challenges. The developments in designing MLIs for renewable energy systems have also been discussed in detail in other reviews such as in [3], where the authors discussed single phase T-type MLI topologies. Asymmetrical MLI structure with fewer components suitably designed for PV system showed increased reliability and decrease in costs [4].

2. Literature review

To demonstrate how MLIs with fewer power switches provide significant improvements, particularly when integrated with renewable energy technologies, a survey of studies is presented for comparison with the current work.

Focusing on the issues of power quality, reference [5] investigated the effects of D-STATCOM and UPQC on cascaded H-bridge nine-level inverters that improve grid interface performance. A new PV-fed asymmetric MLI was developed by [6] to attain a lower total harmonic distortion (THD) level combined with system efficiency. In terms of practical application, more specifically in renewable energy integration, the application of cascaded asymmetrical MLI was further explained in [7]. In addition, an expansive overview of different MLI techniques and control methodologies applied for grid-connected PV systems was analyzed in [8]. An analysis of topologies for grid-connected PV systems, along with observations on trends and future developments, was presented in [9].

New objectives in MLI configurations, for instance, the application of series compensators for power quality enhancement [10], and modified control structures incorporating renewable energy subsystems [11], are indicative of ongoing attempts to improve MLI performance. A grid-connected solar power transfer unit with power quality improvement using an MLI and new design was proposed by [12]. Further development includes better MLI performance for asymmetrical configurations [13] and investigations into different invasive weed optimization techniques focused on operating symmetrical and asymmetrical inverters [14]. On the other hand, a power quality-enhanced resilient approach toward precise control of a grid-integrated solar PV system with an asymmetric 15-level inverter to ensure required robustness against grid issues was put forward in [15]. Empirical studies, including the one by [16], mitigated multiple connections for improving power quality while giving an experimental feel to real-life implementation. Lastly, the authors of [17] addressed specific concerns on newly developed reduced-switch MLIs, especially for renewable energy systems, while stressing cost-effective solutions with detailed discussion and performance comparison. MLIs have become increasingly important due to the need to integrate renewable energy sources efficiently and reliably, particularly in PV systems. Reduced switch MLI topologies analyzed by [18] focused on the use of these topologies in renewable energy systems and drive applications, advancing cost-effectiveness and efficiency. The use of MLIs in grids integrated with renewable energy sources to improve scalability and performance was highlighted and discussed in [19]. An asymmetrical MLI with fewer components fed by PV systems reduced voltage stress and made the system reliable and economic [20]. Meanwhile, an asymmetric MLI topology with a robust fault management strategy for high-reliability applications requiring operational stability was implemented by [21]. The potential of symmetric MLI cascaded H-bridge inverters in efficient renewable energy integration was detailed by [22]. Suggested asymmetrically switched MLIs using PV systems mitigated harmonics [23]. A comprehensive review of MLI advancements, focusing on efficiency and MLI application, was offered by [24]. Performance improvements in asymmetric MLIs for grid-connected solar PV systems, towards better system integration, were studied by [25]. In PV-based MLIs [26], explored harmonic mitigation techniques in order to achieve substantial reductions in THD. In [27], the scope of single and three-phase MLIs along with advanced energy management for renewable energy systems was covered. An innovative MLI design using advanced control structures was presented by [28] to optimize the energy conversion process. Building upon this foundation, the authors in [29] designed a reduced switch MLI topology with no zero-level state, and the results showed improved performance measured in terms of efficiency and system reliability. In the case of solar-fed cascaded MLIs, as suggested by [30], output voltage regulation techniques allowed for significant power quality improvements. Verified by [31], an improved cascaded MLI topology with asymmetric DC sources has shown increased power density and reliability for PV systems. MLI topologies for renewable energy applications were given by [32] to explore their role in intelligent energy systems. In [33], a reduced switch MLI for PV systems that leads to significant improvements in power quality and energy efficiency was demonstrated. Reference [34] reviewed a broad spectrum of MLI designs in PV and trends toward reduced switch topologies with control strategies to balance cost versus performance.

Reference [35] proposed an asymmetrical inverter capable of generating 125 output levels using a reduced switch count, achieving high output resolution with minimal hardware complexity. Additionally, reference [36] reviews high-level asymmetrical MLI topologies, highlighting how advanced designs can obtain a high number of levels without a proportional increase in component count. For instance [37], achieved an 81-level output using only a reduced number of switches. Furthermore, reference [38] provides a comprehensive comparative overview of asymmetrical MLI topologies, some of which exceed 100 levels, enabling beneficial performance trade-offs.

Recent advancements in MLI technology have increasingly focused on balancing structural efficiency with advanced control methodologies to enhance reliability and power quality. Reference [39] addressed the techno-economic aspects of these systems by conducting a quantitative analysis of the reliability and cost functions for a 15-level inverter. Building on the need for robust operational management, performed an extensive investigation into intelligent-based control techniques to mitigate nonlinearities. Specific applications of these intelligent systems were further explored by [40], who analyzed the impact of various ANN algorithms on power quality improvement. In the context of grid integration [41], reviewed the deployment of optimization techniques for grid-tied MLIs, highlighting the critical role of optimized switching in ensuring synchronization. Complementing these control-based improvements [42], proposed a structural innovation involving a modified MLI topology paired with a modified triangular carrier SPWM approach, effectively reducing component count while enhancing the harmonic spectrum.

These studies as a whole highlight advancement in MLI technologies in the form of reduced switch designs, harmonic mitigation, fault management, and advanced control strategies towards stable and efficient renewable integration. This paper models a new single-phase 343-level inverter arrangement with minimum switches using the phase disposition level-shifted PWM (PDLSPWM) controller technique, as shown in Fig. 1, to minimize harmonic distortion while achieving high power outputs.

3. Methodology

The suggested circuit in Fig. 1 illustrates a designed asymmetrical MLI for high performance in industrial applications and the direction of current of some different level is shown in Fig. 2. By employing a special arrangement of asymmetrical DC sources (Vdc) using (1:2:7:14:49:98) Vdc structure, a large number of voltage levels with minimum components is achieved to improve both efficiency and power quality.

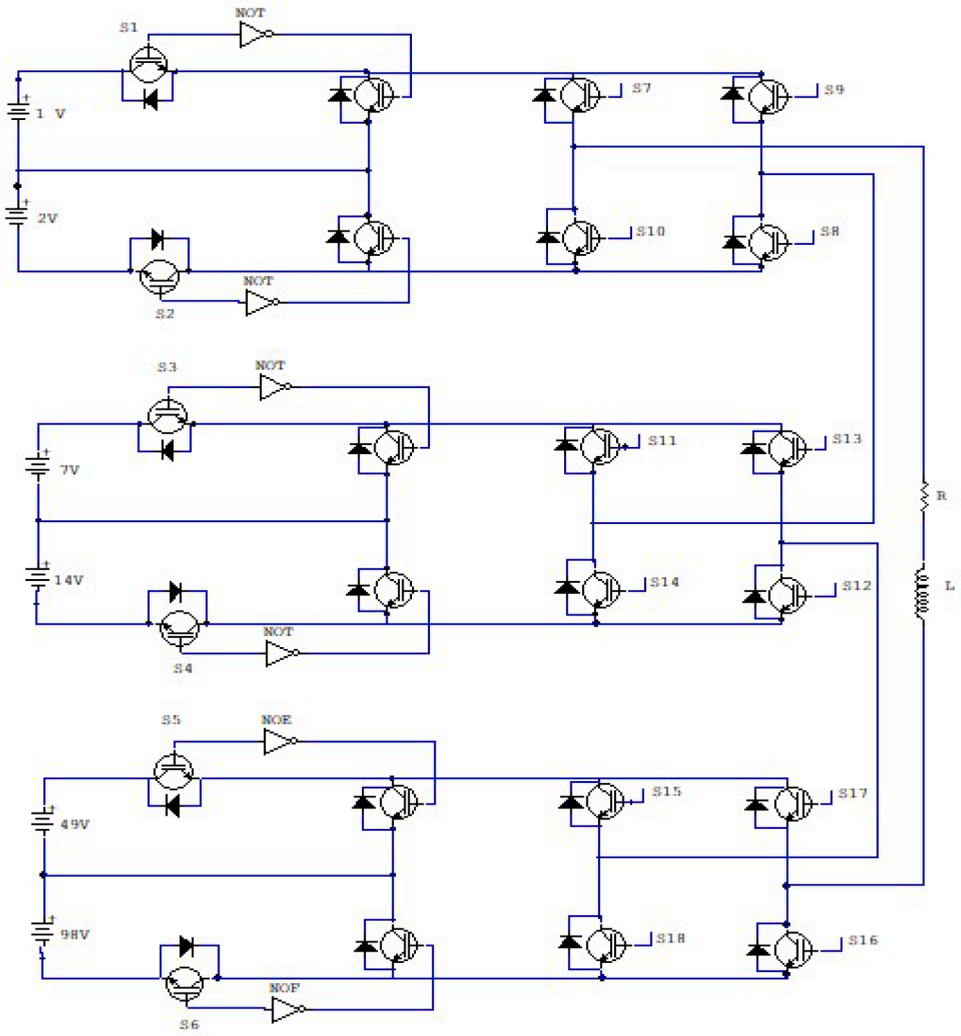


Fig. 1. Circuit diagram for a 343-level asymmetrical multilevel inverter.

Derivation of Asymmetric Voltage Ratio: The specific voltage ratio (1:2:7:14:49:98) is mathematically derived to maximize the number of achievable output voltage levels while minimizing redundant steps and component requirements. The ratio is constructed based on prime factor decomposition using powers of 7 and 2:

First level : $1 = 7^0 \times 2^0$

Second level : $2 = 7^0 \times 2^1$

Third level : $7 = 7^1 \times 2^0$

Fourth level : $14 = 7^1 \times 2^1$

Fifth level : $49 = 7^2 \times 2^0$

Sixth level : $98 = 7^2 \times 2^1$

This geometric progression enables generation of 343 distinct voltage levels (including zero and polarities) through superposition of the six sources. The total number of levels is calculated as:

$N_{levels} = 2 \times (1+2+7+14+49+98)+1 = 2 \times 171+1 = 343$

The selection of base primes 7 and 2 was optimized through comparative analysis with alternative ratios (e.g., 1:2:4:8:16:32 binary, 1:3:9:27:81 ternary). The 1:2:7:14:49:98 ratio achieves superior granularity with fewer redundant voltage steps compared to binary progression (which would require 2^6-1 = 63 levels for 6 sources), while maintaining manageable voltage magnitudes for practical implementation. This optimization directly contributes to the minimal THD achieved (0.32%) by ensuring uniform voltage step distribution. The topology aligns well with batteries and PVs as inputs and the system offers a reliable solution for power quality enhancement as shown in Fig. 1.

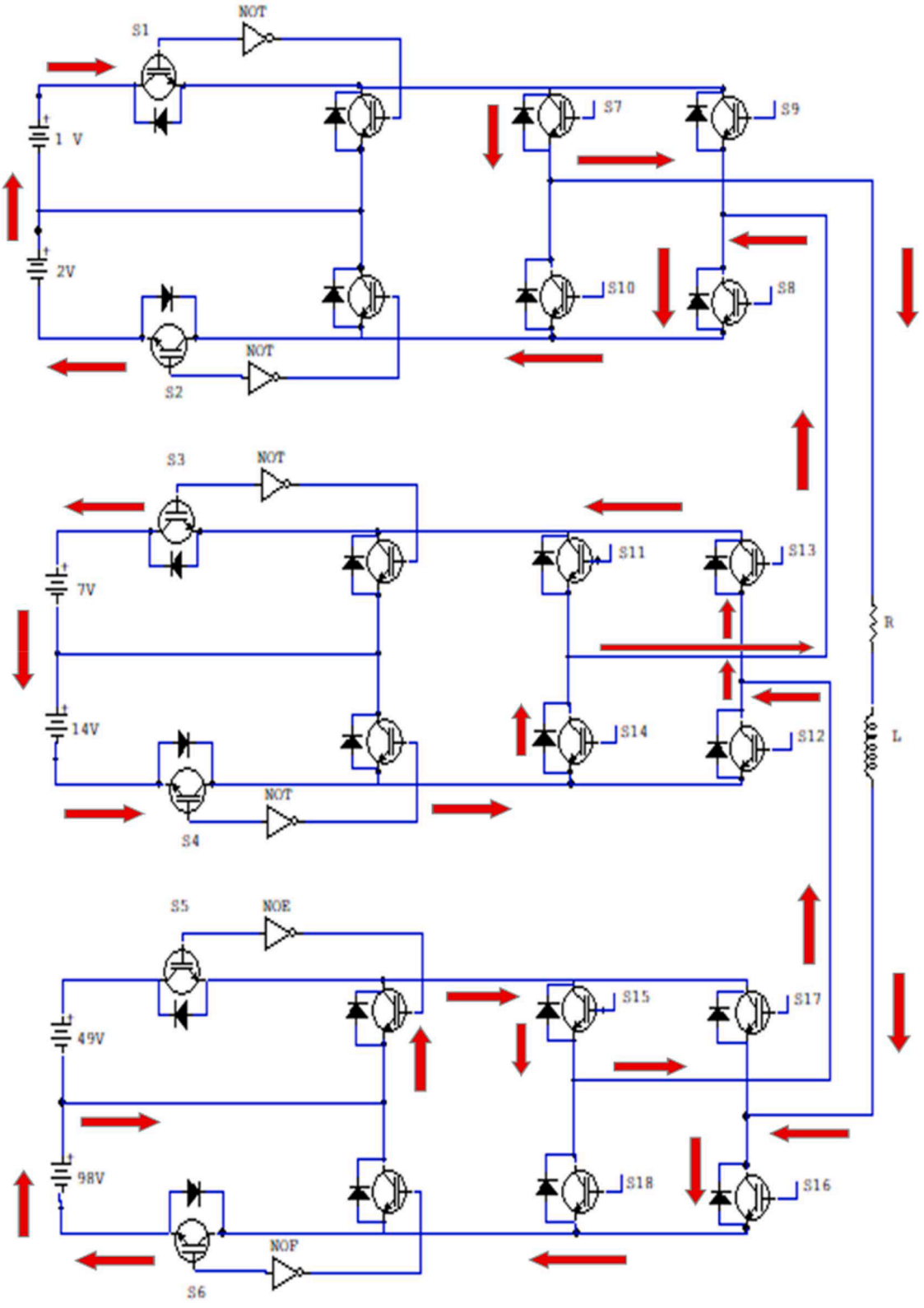
The designed power circuit of the 343-level inverter is designed to generate multiple output voltages according to the structure of (1:2:7:14:49:98)Vdc, which are summed or subtracted by switches at different combinations to get the required output level [28].

Number of withes and DC sources are calculated according to:

$$\text{No. of SW} = (N-1)/19 \quad (1)$$

$$\text{No. of DC source} = (N-13)/55 \quad (2)$$

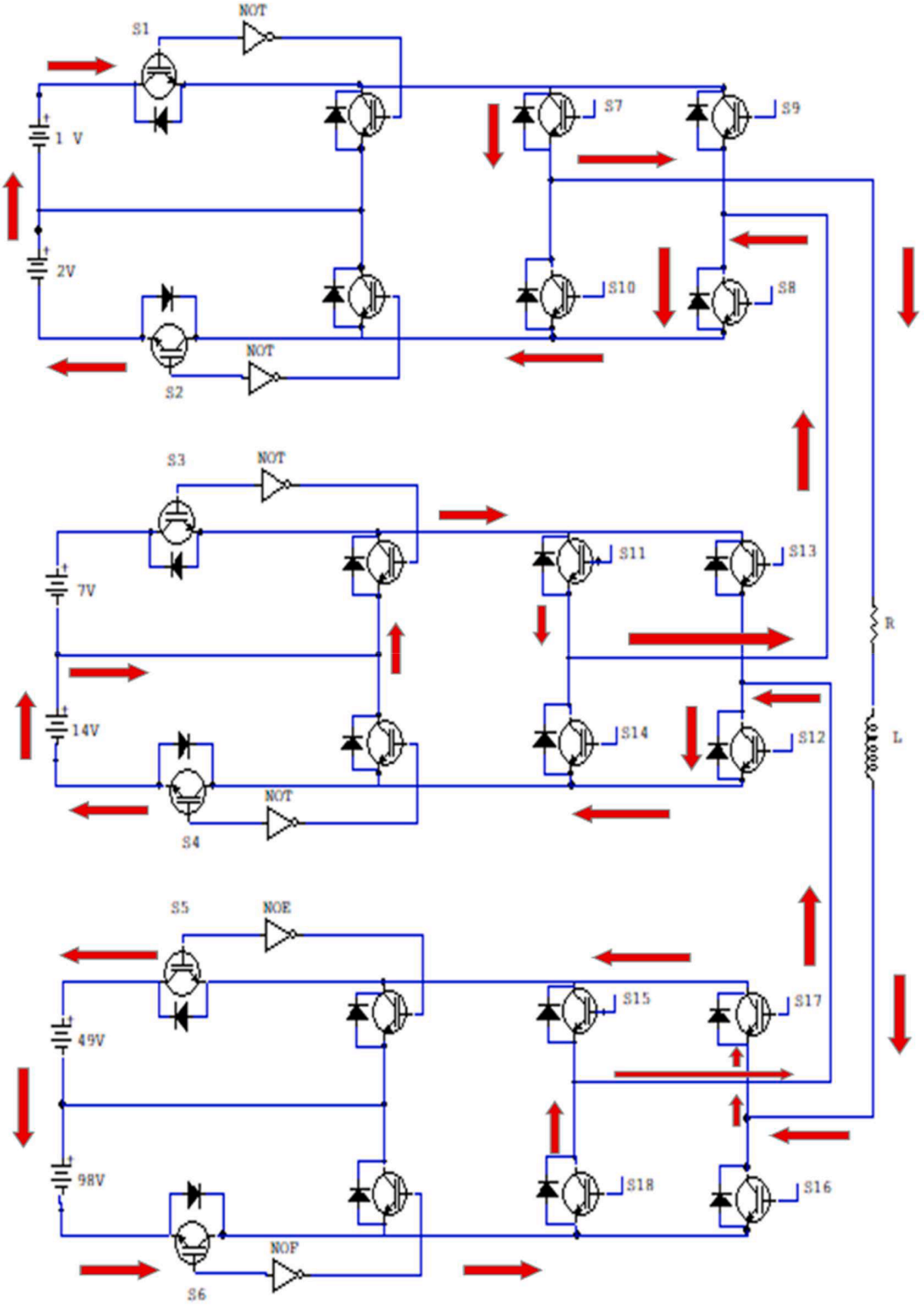
Fig. 2. Selected operation modes showing current paths of 343-level output voltage inverter: (a) Generation of +80 level—switches S1, S2, S7, S8, S11, S12, S15, S16 are ON, creating positive current path through sources 1 V, 2 V, 7 V, 14 V; (b) Generation of −130 level—switches S2, S4, S6, S8, S10, S12, S14, S16, S18 are ON, creating negative current path. Red arrows indicate current direction. These examples demonstrate the switch combination logic for achieving specific output voltages through superposition of asymmetric sources.



(a)

Fig. 2. Current path of 343-level output voltage inverter to produce (a) 80 level (b) −130 level.

Since there are many possible operating patterns to achieve the 343-level output, Table 1 presents some selected switching state patterns of the 343-level inverter based on the voltage source structure of (1:2:7:14:49:98) *Vdc*, while all the switching state patterns are provided in the Appendix section. The proposed power circuit utilizes 18 switches (SWs) and six asymmetrical DC sources to achieve the specified voltage



(b)

Fig. 2. (*continued*).

levels at the load. A switching frequency of 3 kHz was selected as the optimal compromise for this topology, balancing power quality with switching losses. This selection is driven by three key factors: (1) at 3 kHz, the switching resolution is sufficient to effectively reduce Total Harmonic Distortion (THD) and minimize low-order harmonics; (2) while higher frequencies generally improve waveform quality, they significantly reduce converter efficiency due to increased losses; and (3) conversely, lower frequencies would necessitate larger output filter

Table 1
Switching state patterns.

Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18
9	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	0	1	0
10	1	1	1	0	0	0	1	1	0	0	1	1	0	0	1	0	1	0
11	1	1	0	1	0	0	0	0	1	1	1	1	0	0	1	0	1	0
37	0	1	0	1	1	0	1	1	0	0	0	0	1	1	1	1	0	0
39	1	1	1	0	1	0	0	0	1	1	0	0	1	1	1	1	0	0
40	0	1	1	0	1	0	0	0	1	1	0	0	1	1	1	1	0	0
80	1	1	1	1	0	1	1	1	0	0	0	0	1	1	1	1	0	0
81	1	1	0	1	0	1	0	0	1	1	0	0	1	1	1	1	0	0
82	0	1	0	1	0	1	0	0	1	1	0	0	1	1	1	1	0	0
121	0	1	1	1	0	1	1	1	0	0	1	1	0	0	1	1	0	0
122	1	1	1	1	0	1	1	1	0	0	1	1	0	0	1	1	0	0
123	1	1	1	1	1	1	0	0	1	1	0	0	1	1	1	1	0	0
167	1	0	1	1	1	1	0	0	1	1	1	1	0	0	1	1	0	0
168	0	0	1	1	1	1	1	0	1	0	1	1	0	0	1	1	0	0
169	1	0	1	1	1	1	1	1	0	0	1	1	0	0	1	1	0	0

components to manage the increased THD. Therefore, 3 kHz provides the ideal balance between harmonic performance and efficiency for the proposed 343-level inverter operating at medium power levels. This approach allows synthesizing high voltage level with high resolution and minimum harmonic distortion. Safe operation is ensured through complementary switching, which prevents short circuits. The scalability and high performance of the inverter make it suitable for renewable energy systems and industrial applications that can overcome those important power quality and efficiency challenges. the PDLSPWM (Phase-Disposed Level-Shifted Pulse Width Modulation) control technique is a modulation method used in multilevel inverters to generate the appropriate switching signals for the inverter's power devices. This technique divides the total number of voltage levels into phases and then shifts each phase to produce the desired waveform. In comparison to other modulation techniques, such as Sinusoidal PWM (SPWM) and Space Vector PWM (SVPWM), PDLSPWM offers several advantages.

1 **Improved Harmonic Performance**: PDLSPWM helps reduce Total Harmonic Distortion (THD) in both the output voltage and current by optimizing the switching sequence and phase displacement. This leads to higher-quality power with less harmonic content.
2 **Reduced Switching Losses**: The technique minimizes the number of switching events by using level-shifted signals, which helps reduce switching losses in power devices, particularly in high-voltage applications.
3 **Better Voltage Balancing**: It ensures better voltage balancing in multilevel inverters, which is crucial for maintaining the performance and efficiency of the system.
4 **Increased Efficiency**: By improving the voltage waveform quality and reducing the number of switches, PDLSPWM enhances the overall efficiency of the system, making it suitable for both medium- and high-voltage applications.

In summary, PDLSPWM stands out due to its ability to provide high-quality output with reduced harmonic distortion and lower switching losses, making it an ideal choice for multilevel inverters compared to other conventional modulation techniques.

4. Results and discussions

To validate the performance and capabilities of the proposed MLI circuit, MATLAB simulation results are presented for three scenarios with varying input DC voltage sources and power factors (PF):

- First Case: simulated under a per unit system with input voltage of Vdc=1pu using structure of (1:2:7:14:49:98)V and PF of 0.92.
- Second Case: actual DC voltage of (Vdc=40 V) with structure of (40:80:280: 560:1960:3920)V and PF of 0.97.
- Third Case: changing batteries with PV boost circuits as DC sources with structure of (40:80:280: 560:1960:3920)V and PF of 0.92.

The simulations demonstrate the circuit's flexibility and capability to operate under different configurations and input sources.

4.1. First case

In this case the system designed to work with per unit system (1:2:7:14:49:98) volts and power factor of 0.92. The power factor is determined by the RL load characteristics ($R = 30\ \Omega$, $L = 40$ mH), calculated as PF = $\cos[\tan^{-1}(\omega L/R)] = \cos[\tan^{-1}(2\pi \times 50 \times 0.04/30)] = \cos(22.62^{\circ}) = 0.923 \approx 0.92$. The modeling circuit is shown in Fig. 3. Load Parameter Selection: The resistive (R) and inductive (L) load values were carefully selected to represent practical operating conditions while achieving specific power factors and power levels. For Case 1 (per-unit system), $R = 30\ \Omega$ and $L = 40$ mH yield a power factor of 0.92 with moderate power levels (50–1350 VA range), suitable for low-voltage validation. These values create a load impedance angle of 22.6°, representing typical lagging loads encountered in residential and commercial applications. For Case 2 (actual high-voltage system), $R = 700\ \Omega$ and $L = 500$ mH produce a power factor of 0.97 with higher power levels (3.4–98 kVA), appropriate for medium-voltage grid-connected applications. The L/R ratio was chosen to ensure sufficient inductive filtering effect while maintaining manageable voltage drop and reactive power flow. Table 2 shows selected levels with analysis of the harmonic distortion and power quality changes with the increase in voltage levels to reach the proposed 343-level inverter output. The system is designed to produce any required output voltage levels. The bold highlighted selected levels in the Table 2 are chosen and plotted to show the output voltage and current waveforms with their frequency spectrum (FFT). This table summarizes the total harmonic distortion of the output voltage (THDVo) and current (THDIo), as well as the apparent power (S), real power (P), reactive power (Q), and distortion power (D).

The produced voltage and current with its FFT analysis of the 63, 133, 203, 273 and 343-level inverter suggested in this paper using PDLSPWM technique are presented in Figs. 4–8, respectively. The THD_{Vo} values for the selected levels are 2.2329%, 1.1175%, 0.71215%, 0.44665%, and 0.32422%, respectively. While the THD_{Io} values are 2.2236%, 1.1288%, 0.585%, 0.3377%, and 0.22506%. These results show that the THD has been improved by increasing the voltage levels. Fig. 9 illustrates the THD_{Vo} and THD_{Io} values at different levels. These outcomes are supported by the distortion power waveform illustrated in Figure (10d). The S, P, and Q waveforms illustrated in Fig. 10(a, b, and c) explains that these powers rise as voltage levels rise. The whole results confirm the efficiency of the proposed MLI circuit and controller.

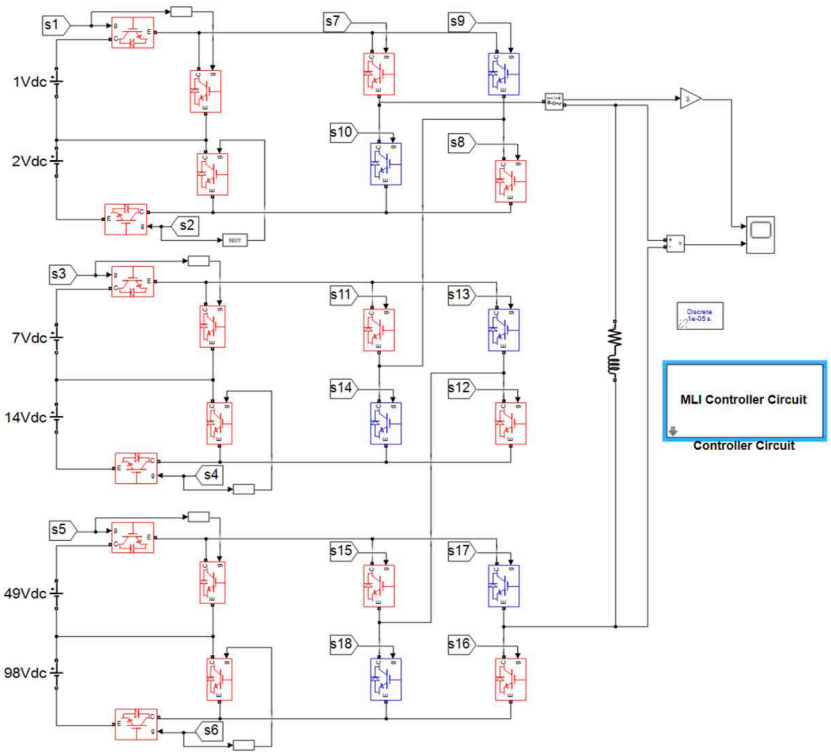


Fig. 3. Design modeling of the proposed 343-level inverter supplied by battery DC sources.

Table 2
Simulation result of voltage and current distortions, and powers.

PF=0.92 R = 30 ohms L = 40 mH			
Level	THDvo	THDio	S P Q D
63	**2.2329**	**2.2236**	**49.0706 45.2583 18.9578 0.4613**
77	1.9465	1.9638	72.3737 66.7513 27.9626 0.5611
91	1.6906	1.6874	100.2321 92.4450 38.7286 0.6986
105	1.4128	1.4397	132.6834 122.3753 51.2703 0.7247
119	1.2447	1.2566	169.5112 156.3410 65.5044 0.8329
133	**1.1175**	**1.1288**	**210.7882 194.4105 81.4577 0.9277**
147	1.014	1.0211	256.9001 236.9386 99.2808 1.0471
161	0.91542	0.92179	307.3332 283.4515 118.7756 1.1332
175	0.88375	0.79084	360.5329 332.5130 139.3440 1.5285
189	0.80902	0.68428	418.6375 386.1002 161.8062 1.6548
203	**0.71215**	**0.585**	**481.9941 444.5301 186.3016 1.7169**
217	0.64896	0.52882	549.8448 507.1052 212.5331 1.8066
231	0.58671	0.47022	622.2888 573.9156 240.5425 1.8925
245	0.54051	0.42809	699.2092 644.8535 270.2843 1.9801
259	0.49436	.38332	780.8167 720.1138 301.8386 2.0703
273	**0.44665**	**0.3377**	**866.8151 799.4235 335.0909 2.1443**
287	0.42425	0.31368	957.5022 883.0551 370.1605 2.3120
301	0.39598	0.29125	1052.5 970.7 406.9 2.4
315	0.37064	0.2674	1151.9 1062.3 445.3 2.5
329	0.34685	0.24365	1256.1 1158.4 485.6 2.6
343	**0.32422**	**0.22506**	**1348.8 1243.9 521.5 2.7**

4.2. Second case

In this case, the system designed to work with actual DC voltages of (40: 80:280:560:1960:3920)V and PF of 0.97. This power factor corresponds to the RL load (R = 700 Ω, L = 500 mH), calculated as PF = cos [arctan(2π × 50 × 0.5/700)] = cos(12.86°) = 0.975 ≈ 0.97. Table 3 shows selected levels with analysis of the harmonic distortion and power quality changes with the increase in voltage levels to reach the proposed 343-level inverter output. The system is designed to produce any required output voltage levels. The highlighted levels shown in the Table 3 are chosen and plotted to show the output voltage and current waveforms with their FFTs. This table shows the THD_{Vo} and THD_{Io}, S, P, Q, and D values.

The voltage and current output waveforms with their FFTs at different levels using PDLSPWM technique are presented in Figs. 11–15, respectively. The THD_{Vo} values for these levels are 2.4042%, 1.1357 %, 0.72424 %, 0.44623%, and 0.32414%, respectively. While the THD_{Io} values are 2.2914%, 1.1106%, 0.6413%, 0.37394%, and 0.25682%. These results show that the THD has been improved by increasing the voltage levels. Fig. 16 demonstrates the THD_{Vo} and THD_{Io} at different voltage levels. These results are supported by the distortion power shown in Fig. 17(d). The S, P, and Q power waveforms illustrated in Fig. 17(a, b, and c) explain that these powers rise as voltage levels rise. The whole results confirm the efficiency of the designed power circuit and controller. To check effectiveness of the system at transient and steady state conditions, the suggested circuit is tested to produce different output voltage and current levels as explained in Fig. 18. The inverter enhances the voltage levels step by step from 49 levels to 343 levels with a step size of 32 levels every 0.2 s.

To validate the novelty, point of the suggested power circuit and controller, the system evaluates the transient response of the output voltage and current over a time period of interest. The inverter enhances the voltage levels step by step from 49 levels to 343 levels with a step size of 32 levels every 0.2 s. Fig. 18 show that it functions appropriately at different levels and at different times on a continuous basis.

4.3. Third case

In this situation, the batteries are changed by PVs that produce outputs of (40:80:280: 560:1960:3920)V. The system with PF of 0.92 is shown in Fig. 19(a). The PV-Boost model and controller system is explained in Fig. 19(b). The outcomes confirm that the inverter can offer good quality power with a very low level of THD at the output,

The PV-Boost model and controller system is explained in Fig. 19(b). The boost converter operates with a switching frequency of 20 kHz, featuring an inductor L = 2.5 mH, capacitor C1 = 470 μF, and capacitor C3 = 100 μF. The MPPT control employs the Perturb and Observe (P&O)

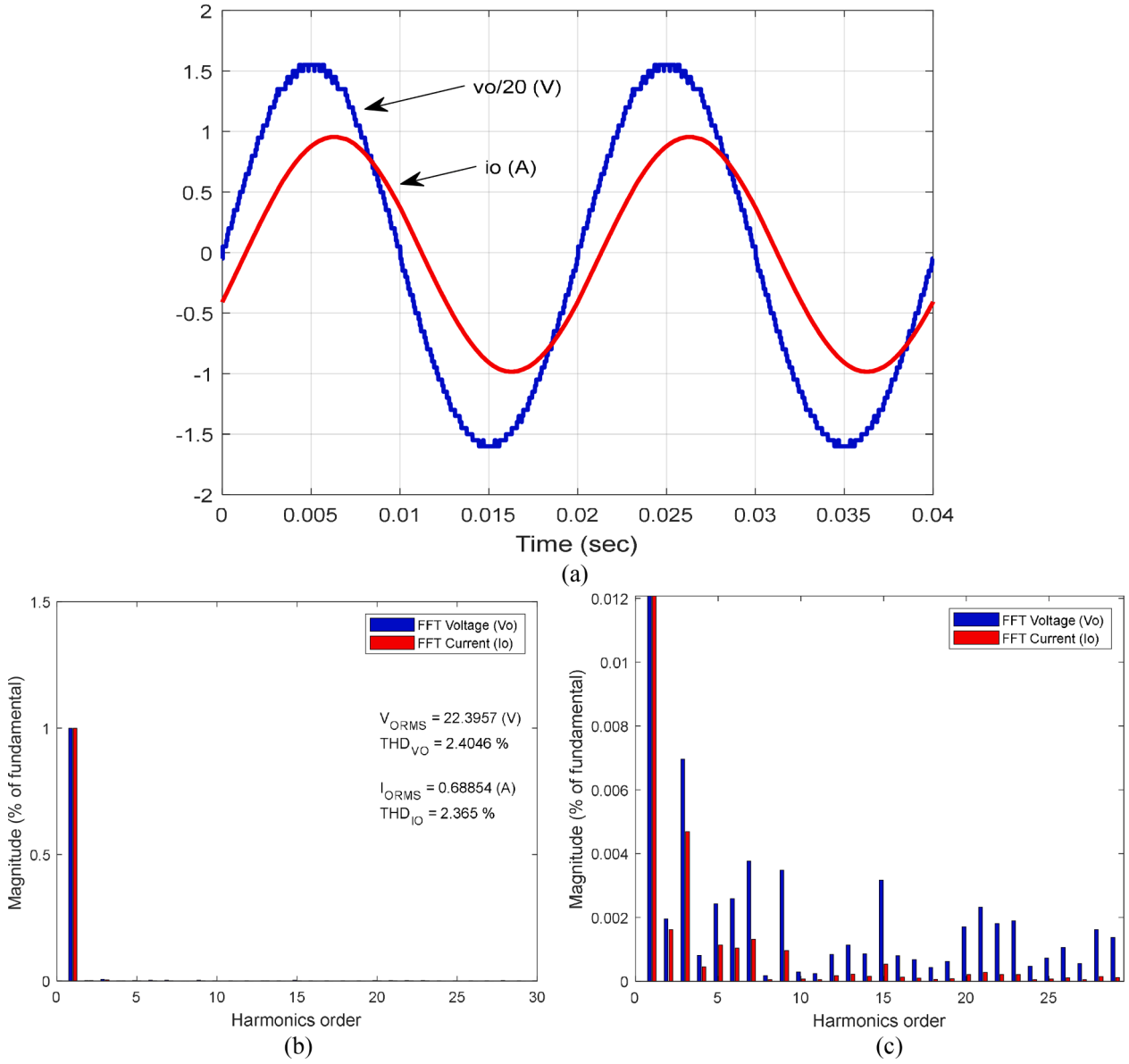


Fig. 4. 63-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

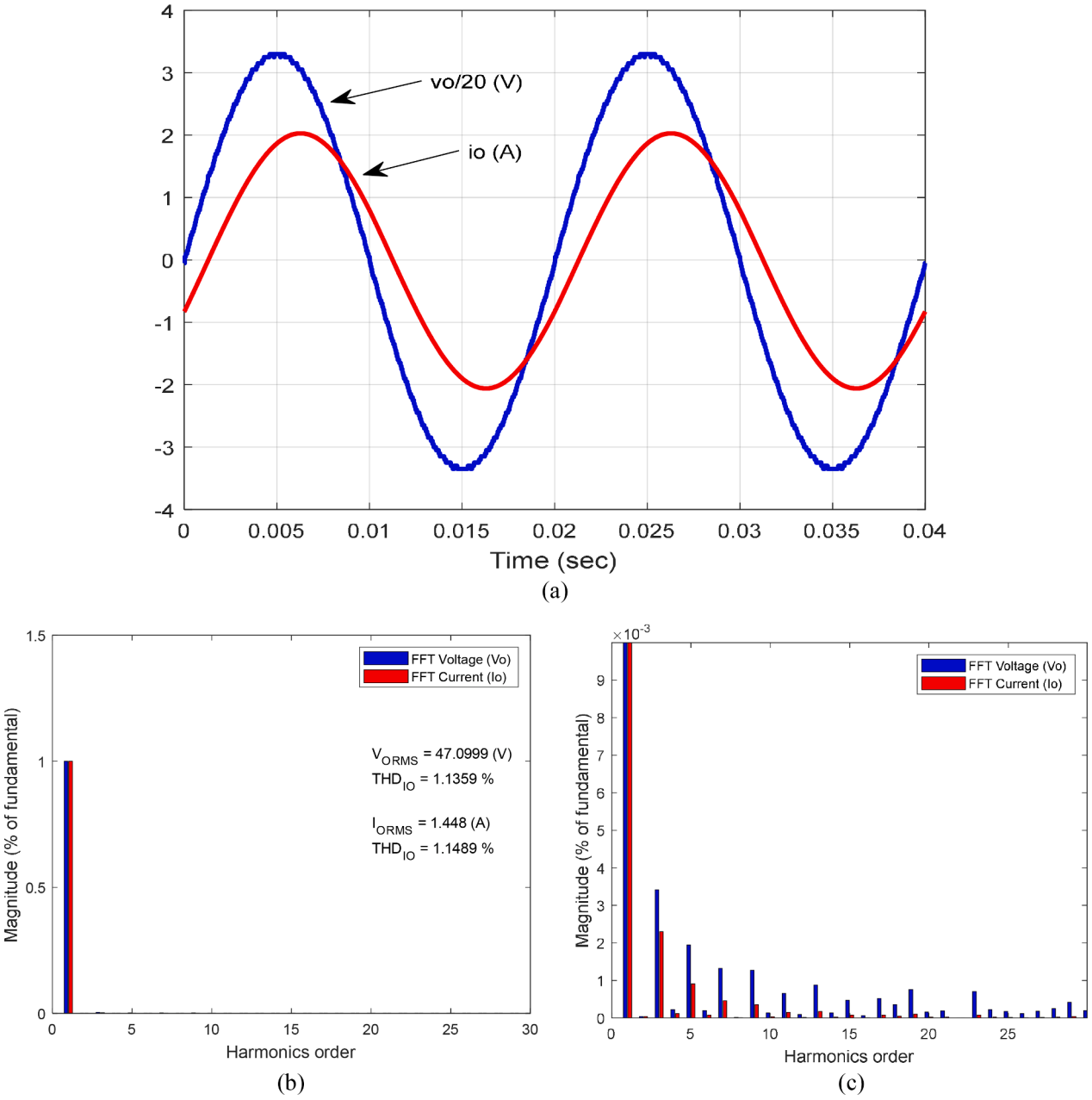


Fig. 5. 113-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

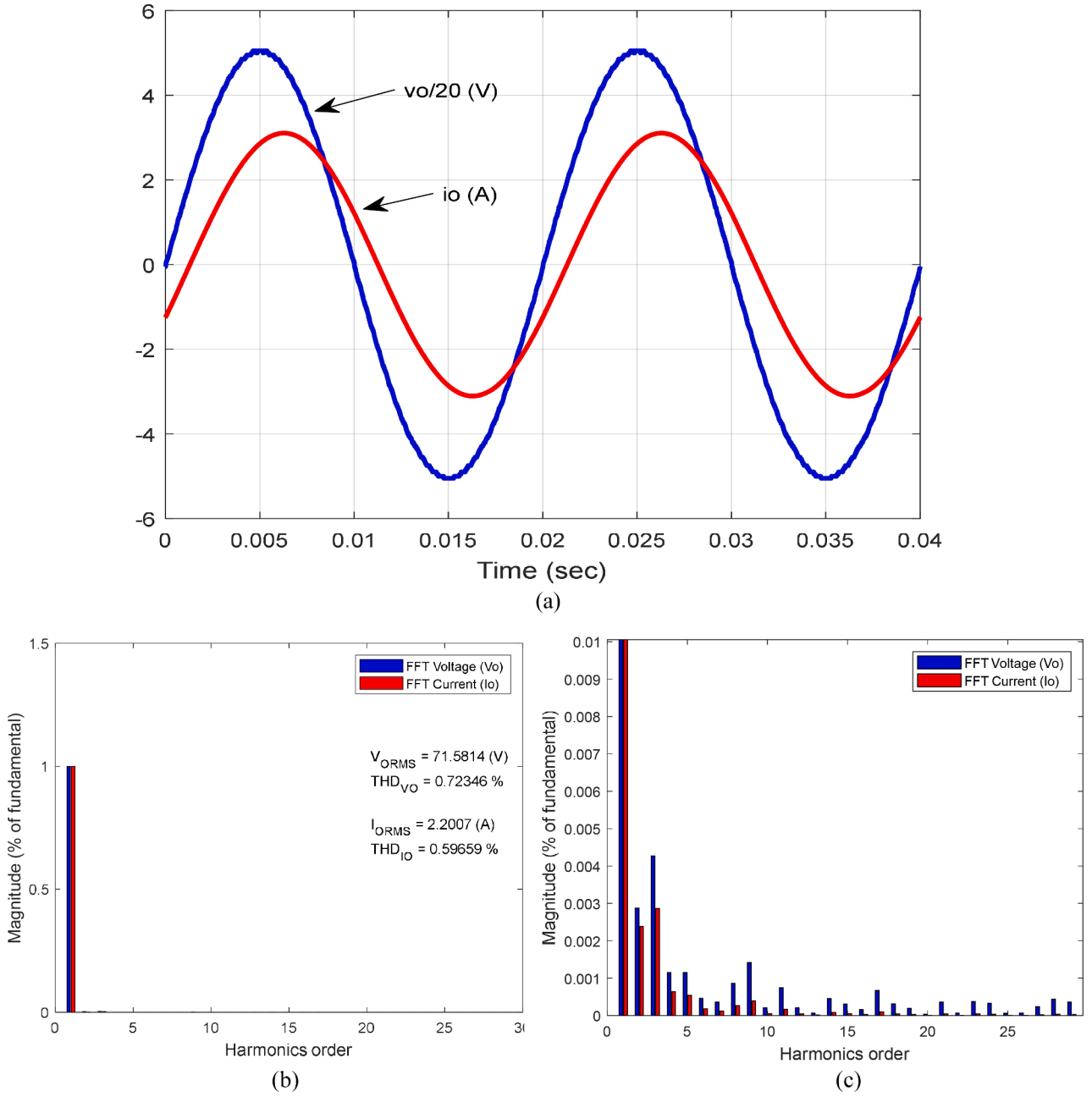


Fig. 6. 203-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

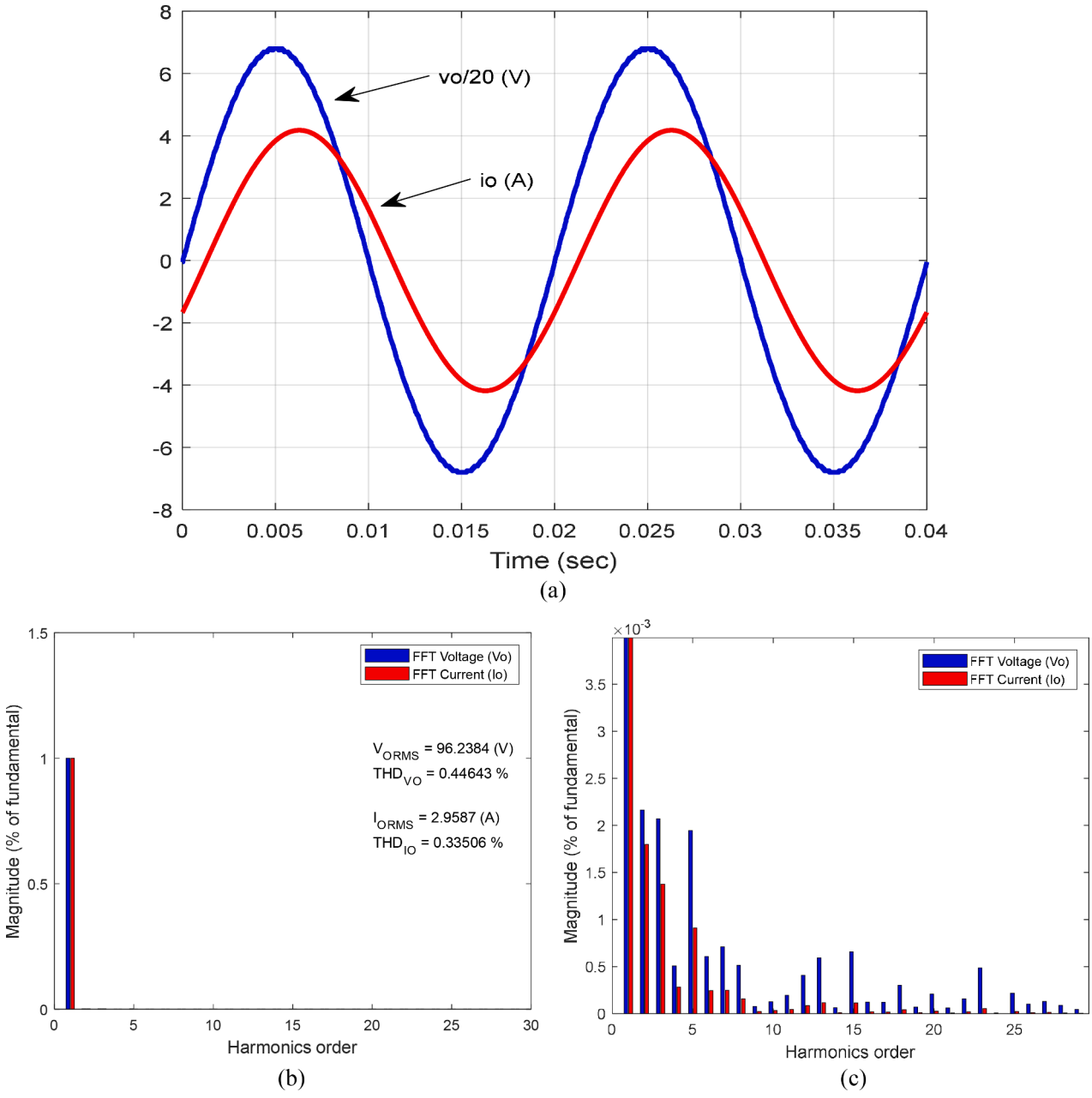


Fig. 7. 273-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

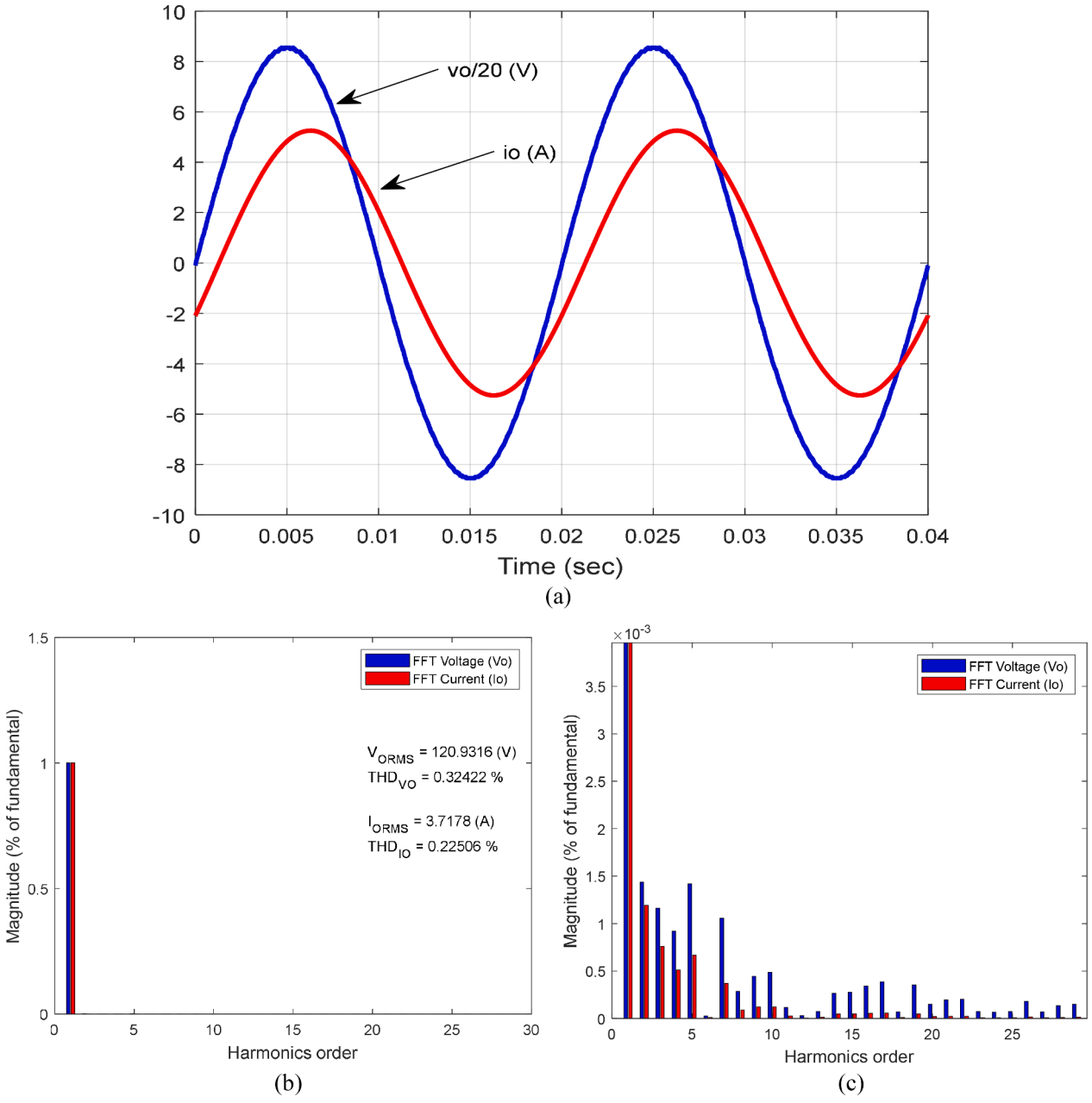


Fig. 8. 343-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

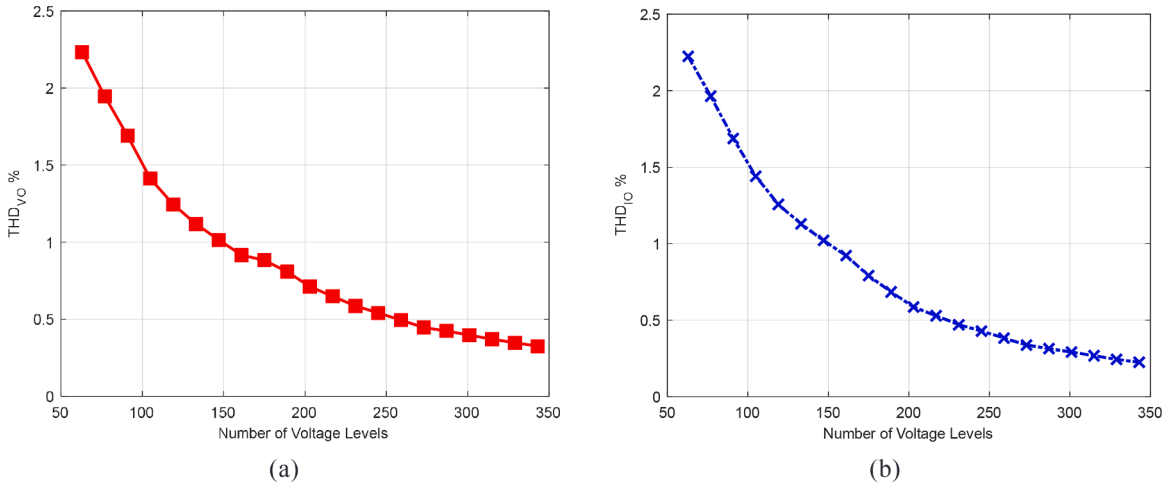


Fig. 9. THD of the output (a) voltage and (b) current at different voltage levels.

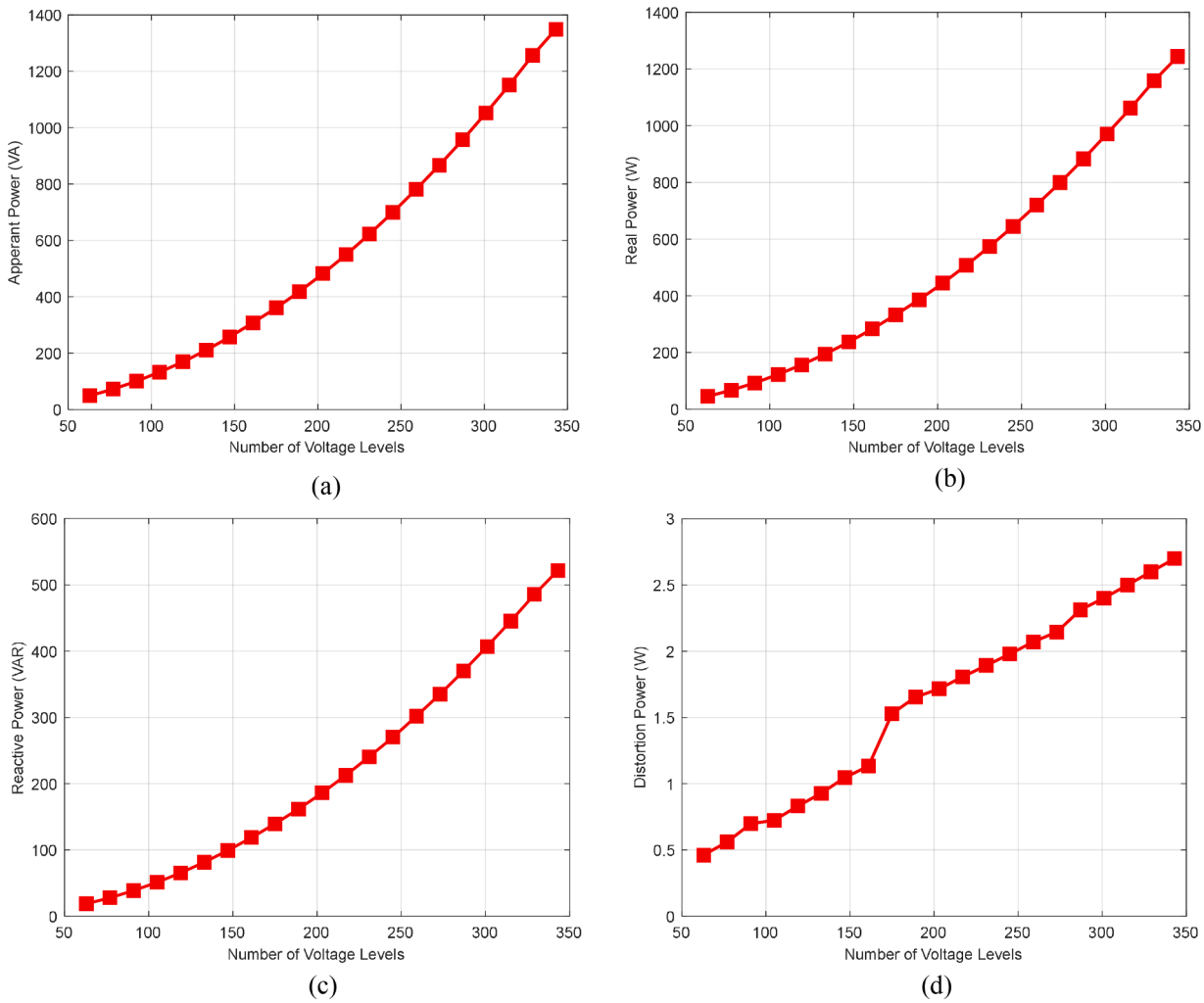


Fig. 10. (a) Apparent power, (b) real power, (c) reactive power, and (d) distortion power.

algorithm to track the maximum power point under varying irradiance and temperature conditions. The boost converter's duty cycle (D) is adjusted according to the voltage error between the reference voltage (Vdcref) and the measured PV voltage, processed through a PI controller with gains Kp = 0.5 and Ki = 25. The mathematical relationship governing the boost operation is given by:

$$V_{boost} = \frac{V_{pv}}{1 - D}$$

where *VPV* represents the PV module output voltage and D is the duty cycle. The MPPT algorithm continuously perturbs the operating voltage

Table 3
Simulation result of voltage and current distortions, and powers.

PF= 0.97 R = 700 ohms L = 500 mH			
Level	THD_{Vo}	THD_{Io}	S P Q D
63	2.4042	2.2914	3357 3275.3 735.2 32.6
77	2.0224	1.9612	4990.2 4868.9 1092.9 38
91	1.731	1.6689	6972.9 6803.4 1527.3 47.4
105	1.4372	1.4062	9274.8 9049.4 2031.6 48
119	1.2459	1.2109	11,905 11,616 2608 54
133	1.1357	1.1106	14,851 14,490 3253 61
147	1.0288	1.0047	18,149 17,708 3976 68
161	0.92552	0.90154	21,761 21,232 4768 74
175	0.88191	0.80974	25,592 24,970 5608 90
189	0.81812	0.73403	29,757 29,034 6521 96
203	0.72424	0.6413	34,301 33,467 7517 101
217	0.65375	0.57796	39,186 38,233 8588 103
231	0.59308	0.5144	44,397 43,318 9731 113
245	0.54093	0.46943	49,936 48,722 10,946 115
259	0.49155	0.4179	55,801 54,444 12,232 123
273	0.44623	0.37394	62,005 60,497 13,593 128
287	0.42006	0.35127	68,529 66,862 15,024 134
301	0.39315	0.3224	75,393 73,559 16,530 145
315	0.36576	0.29656	82,576 80,567 18,106 152
329	0.35002	0.28264	90,074 87,882 19,751 159
343	0.32414	0.25682	97,905 95,522 21,469 166

and observes the power change to maintain operation at the maximum power point, ensuring optimal energy extraction from the PV arrays under all environmental conditions. Voltage Balancing Control: For DC battery configurations, the voltage balancing is inherently ensured by selecting fixed source values according to the asymmetric ratio (1:2:7:14:49:98) or actual values of (40:80:280:560:1960:3920)V. For PV-fed implementations, active voltage balancing is achieved through the boost converter control loop shown in Fig. 19(b). Each PV-boost subsystem incorporates voltage feedback where the measured boost output voltage (V_{boost}) is compared against its reference value (V_{dcref}) corresponding to the required ratio. The PI controller generates the appropriate duty cycle adjustment to compensate for PV voltage variations caused by irradiance and temperature changes. This ensures that the DC-link voltages maintain their precise ratios regardless of environmental conditions, enabling stable 343-level output generation. The individual MPPT controllers for each PV string further ensure maximum power extraction while maintaining voltage balance. The outcomes confirm that the inverter can offer good quality power with a very low level of THD at the output, which makes it suitable for current and future energy systems, including smart grids, isolated power systems, and renewable energy interconnection. The (V-I) and (P-V) characteristics of the PV modules are shown in Fig. 20. The 343-level inverter's output using PDLSPWM technique is illustrated in Fig. 21. The THD_{Vo} and THD_{Io} are calculated to be 0.9328% and 0.54122%, respectively.

4.4. Fourth case: dynamic performance under variable environmental conditions

To comprehensively evaluate the robustness of the proposed 343-level inverter under realistic operating scenarios, this section presents simulation analysis exploring various cases based on expanded environmental and load conditions. The results were categorized by irradiation (Ir), temperature (T), and RL load conditions, allowing detailed assessment of their specific impacts on key performance metrics: output voltage, distortion power, and total harmonic distortion (THD) of output voltage (THDvo) and output current (THDio).

4.4.1. 343-level inverter at variable irradiation and constant temperature (25 °C) with fixed output voltage

This case evaluates the effect of varying solar irradiation levels (1000, 800, 600, and 200 W/m^2) on a 343-level inverter system operating at a fixed temperature of 25 °C with fixed output voltage conditions as shown in Fig. 22. With MPPT active, the PV system extracts maximum available power at each irradiation level. The analysis focuses on how power components respond to changes in irradiation despite voltage stability. Increased irradiation improves real and apparent power and reduces distortion power, while lower irradiation has the opposite effect. The output voltage and current waveforms under different irradiation conditions, along with THD of the output voltage and current, remain equal to or <1% as indicated in Figs. 23 and 24.

a) **Ir= 800 W/m^2, PF= 0.9827**

S, P, Q, D = [172,500 169,520 31,950 260]

a) **Ir= 200W/m^2, PF= 0.9827**

S, P, Q, D = [172,510 169,520 31,960 270]

4.4.2. 343-level inverter at variable temperature and constant irradiation 1000 W/m^2 with fixed output voltage

In this case, the performance of the 343-level inverter is assessed under fixed irradiation (1000 W/m^2) while varying temperature (15 °C, 20 °C, 30 °C, 35 °C and 40 °C) that maintaining a fixed output voltage throughout as displayed in Fig. 25. MPPT control ensures optimal energy extraction from the PV source. The purpose is to examine the influence of temperature variation on power delivery and quality. As temperature rises, both real and apparent power decrease, while distortion and reactive power tend to increase, reflecting the typical behavior of PV modules under thermal stress. The output voltage, current in different temperature and THD of the output voltage still <2% and for current less than or equal 1% as indicated in Figs. 26 and 27.

a) ***T* = 20 °C, PF= 0.9826**

S, P, Q, D = [243,380 239,140 45,120 03,020]

a) ***T* = 35 °C, PF= 0.9827**

S, P, Q, D = [226,630 222,700 42,010 1920]

The simulation results demonstrate that optimal inverter performance is achieved under conditions of higher irradiation, moderate to lower temperatures, and relatively higher load impedances. These factors collectively ensure higher output voltage, reduced distortion power, and minimized THD. Understanding the influence of these parameters is critical for designing and optimizing inverter systems for efficient renewable energy applications.

The performance of the designed power circuit and controller is compared with others as explained in Table 4. The comparisons are made on the basis of levels, number of switches, number of diodes used, source type of input and the THD_{Vo} and THD_{Io}. This proposed circuit is appropriate especially in the new and renewable energy systems, and industrial applications that require high precision in performance and the quality of power delivered such in large scale renewable energy integration, smart grid systems etc. The comparison demonstrates that the proposed topology achieves the highest number of output levels (343) with the minimum switch count (18) among comparable high-

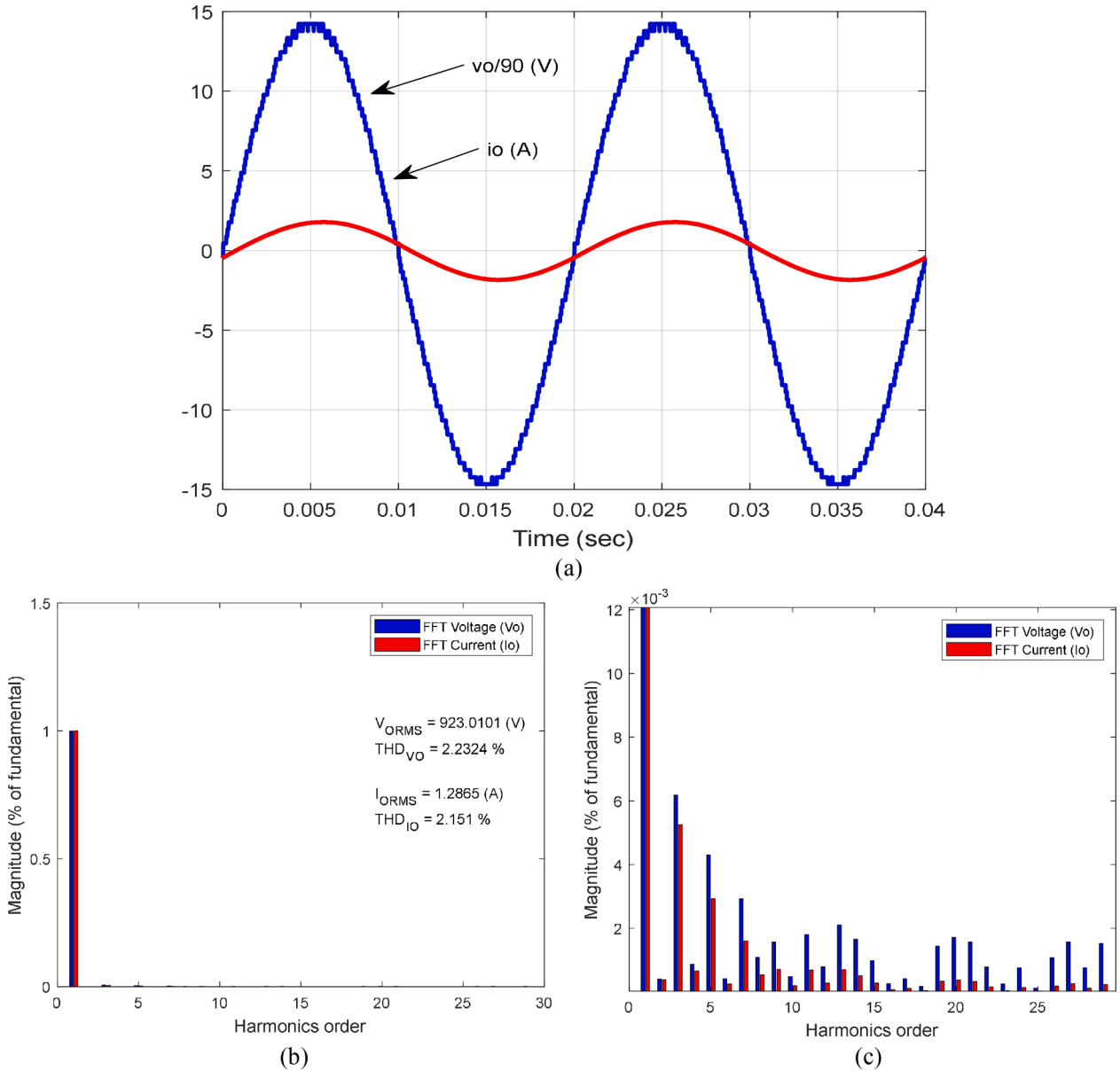


Fig. 11. 63-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

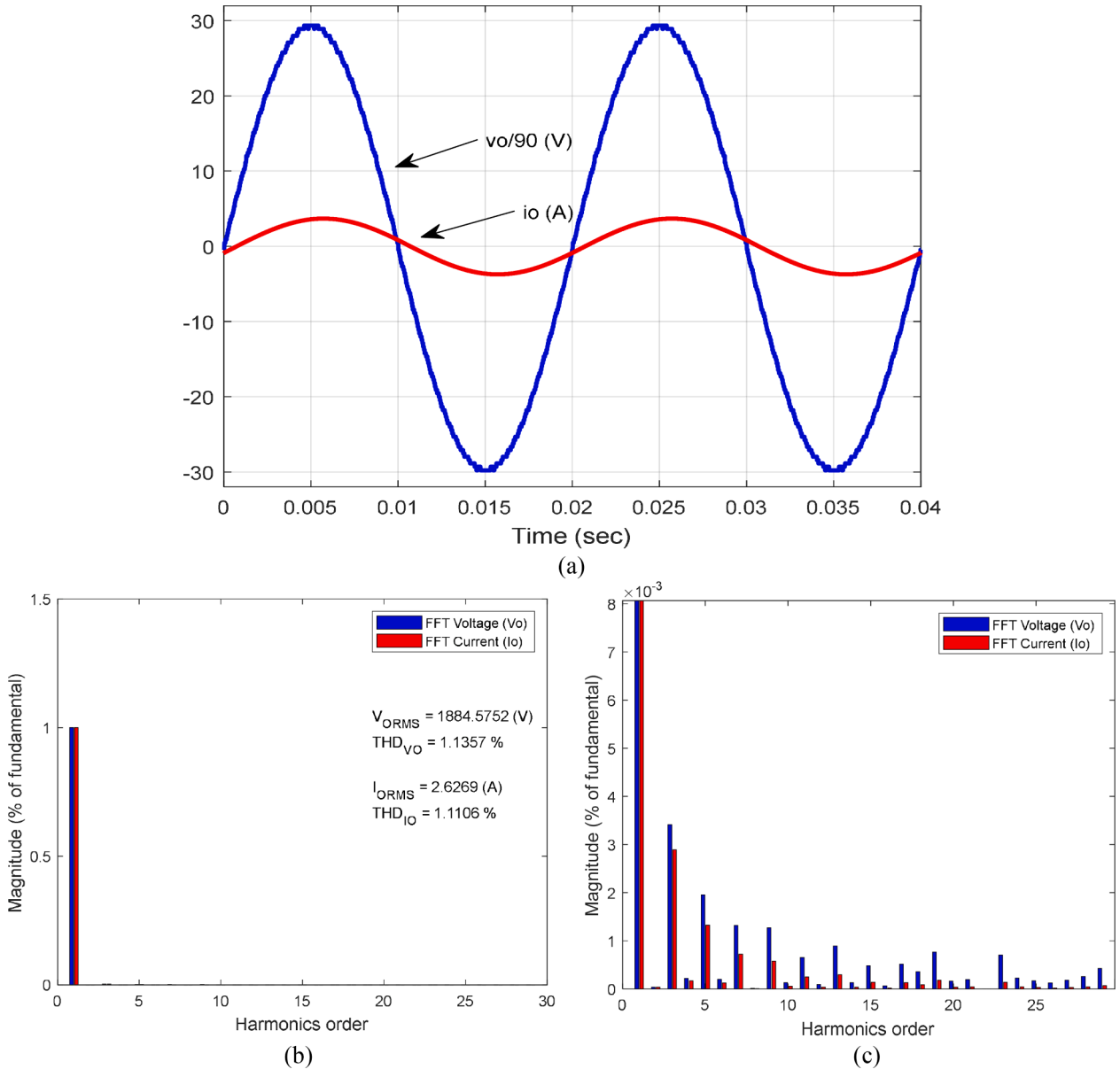


Fig. 12. 133-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

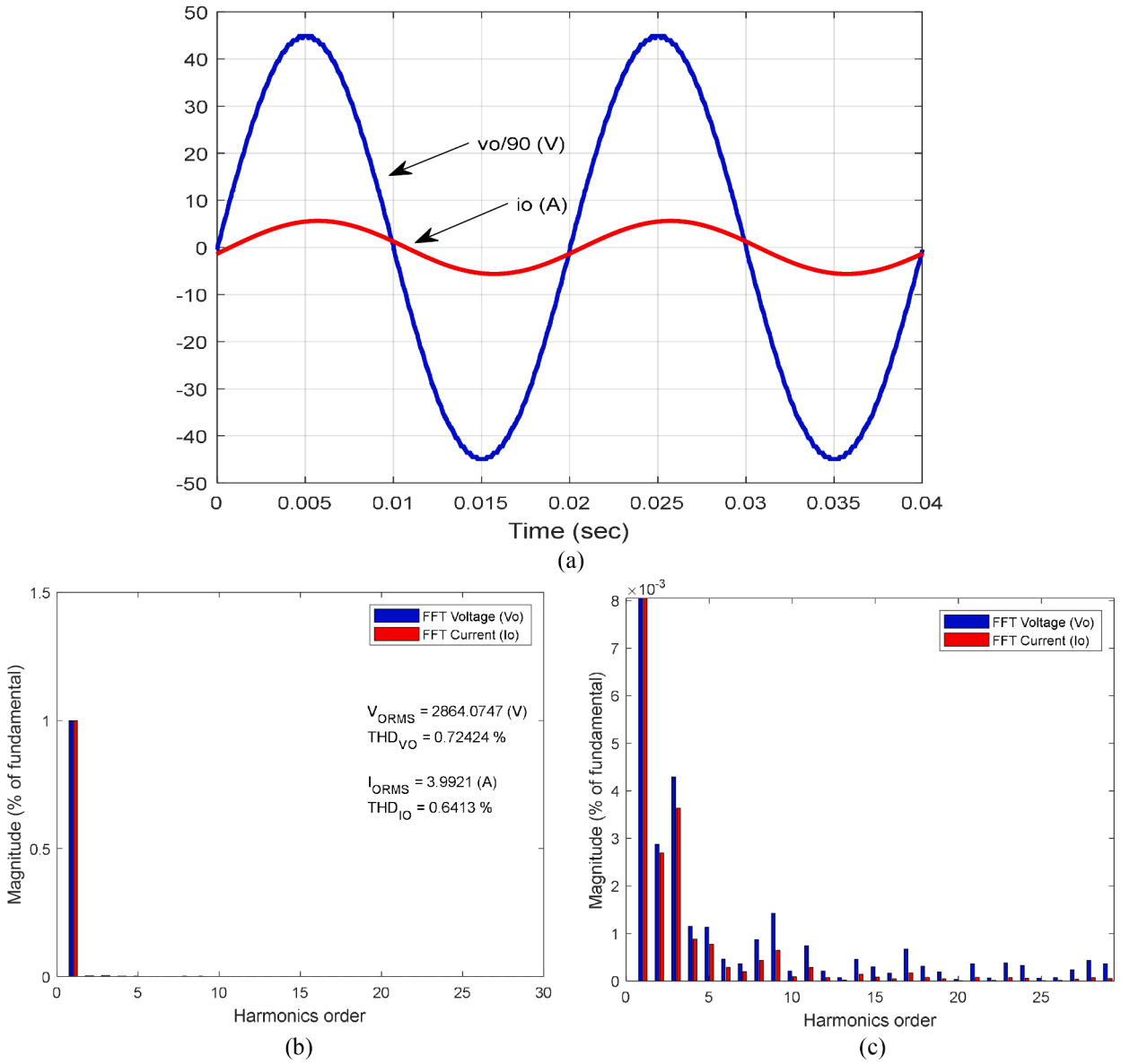


Fig. 13. 203-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

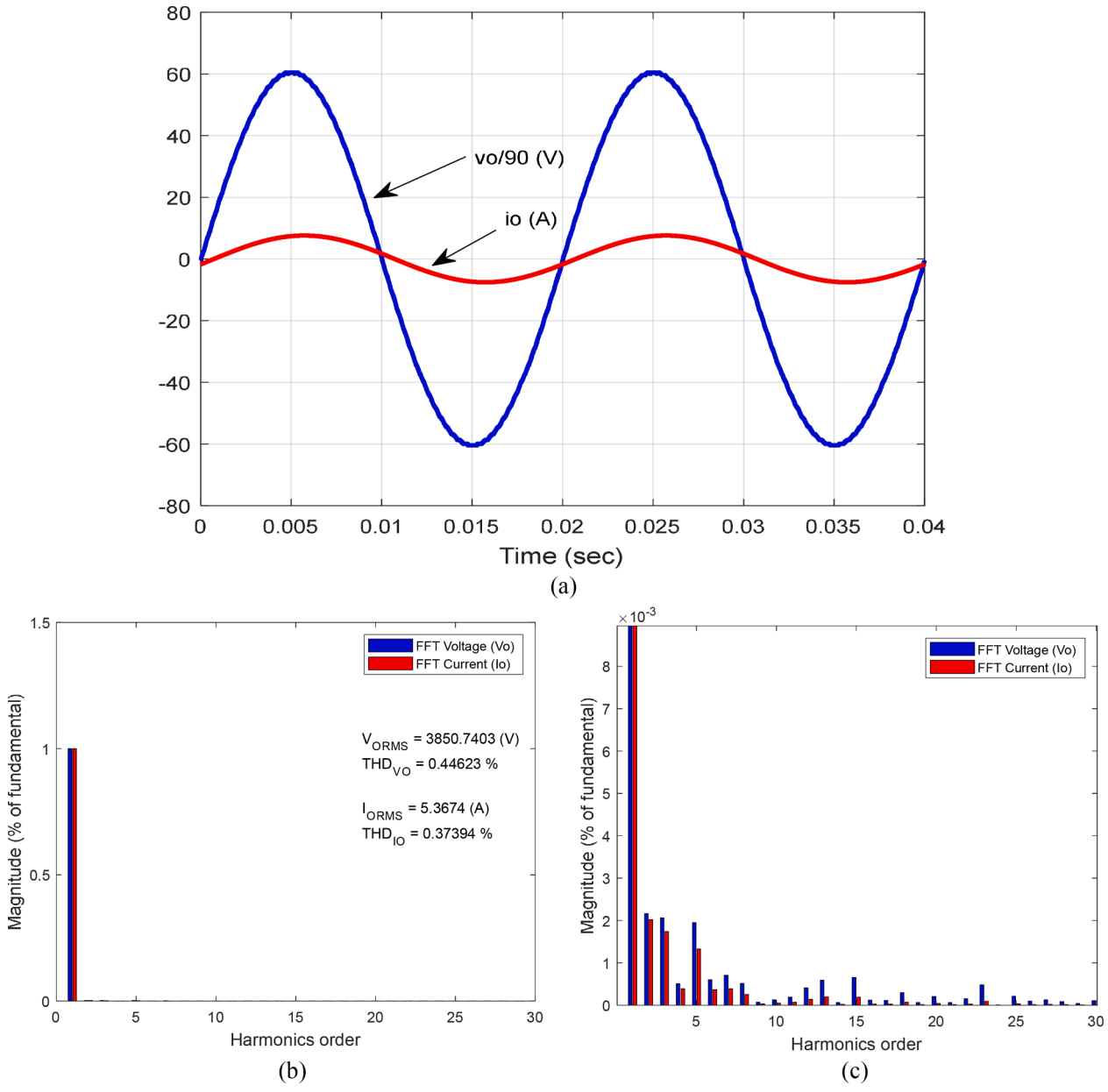


Fig. 14. 273-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

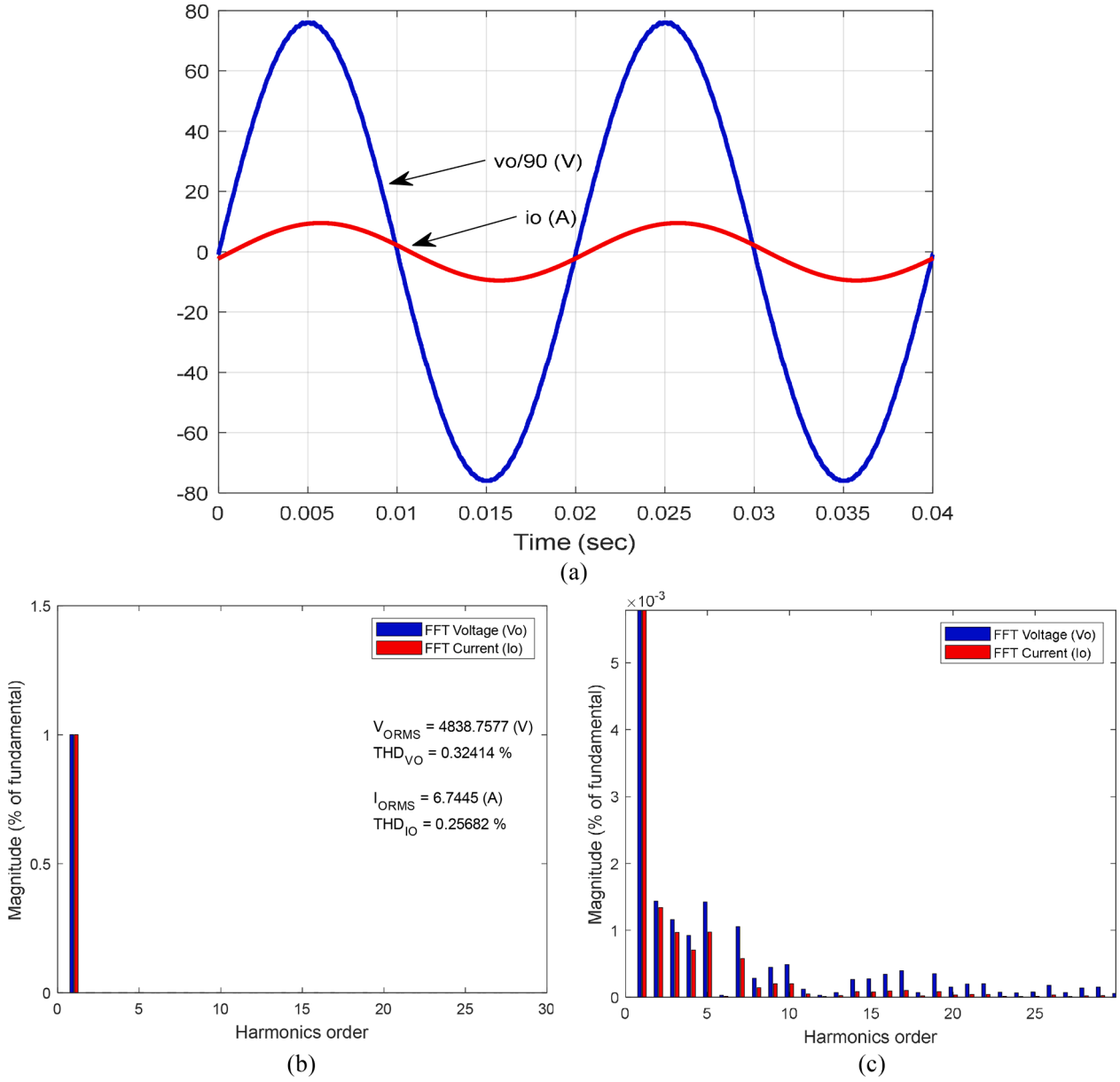


Fig. 15. 343-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

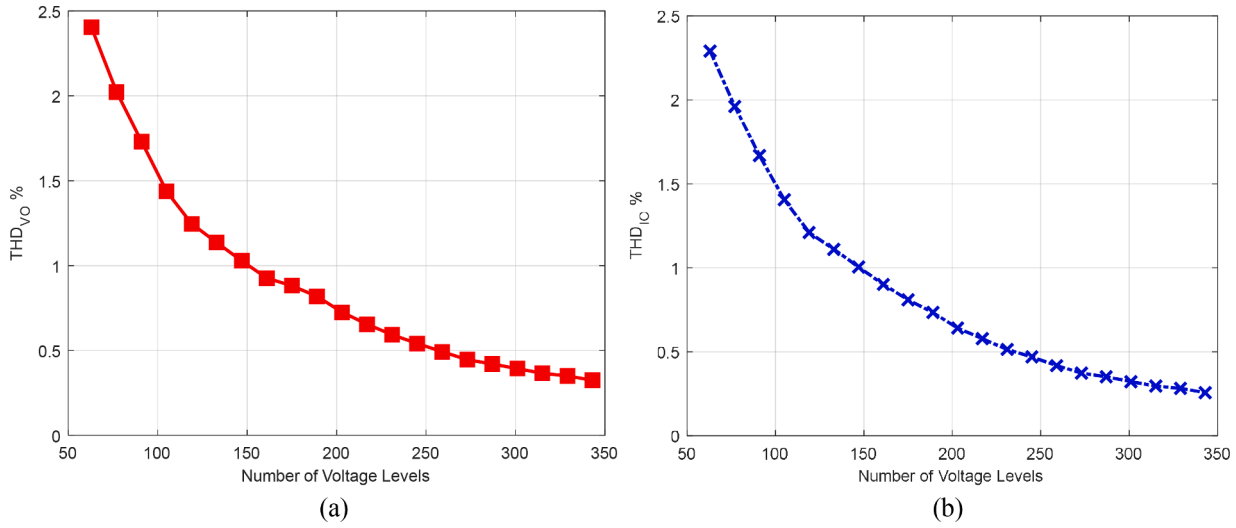


Fig. 16. THD of the output (a) voltage and (b) current at different voltage levels.

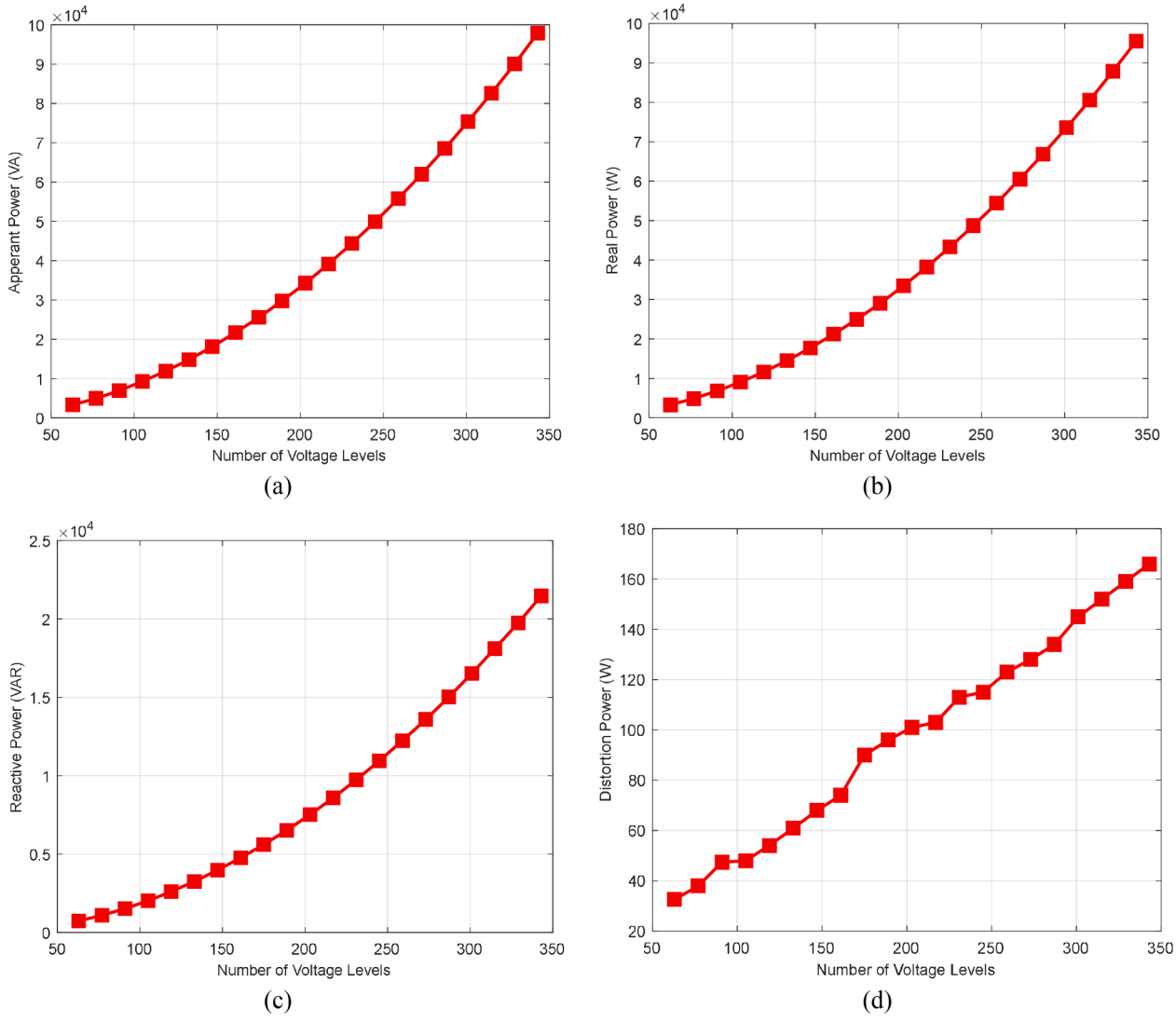


Fig. 17. (a) Apparent power, (b) real power, (c) reactive power and (d) distortion power.

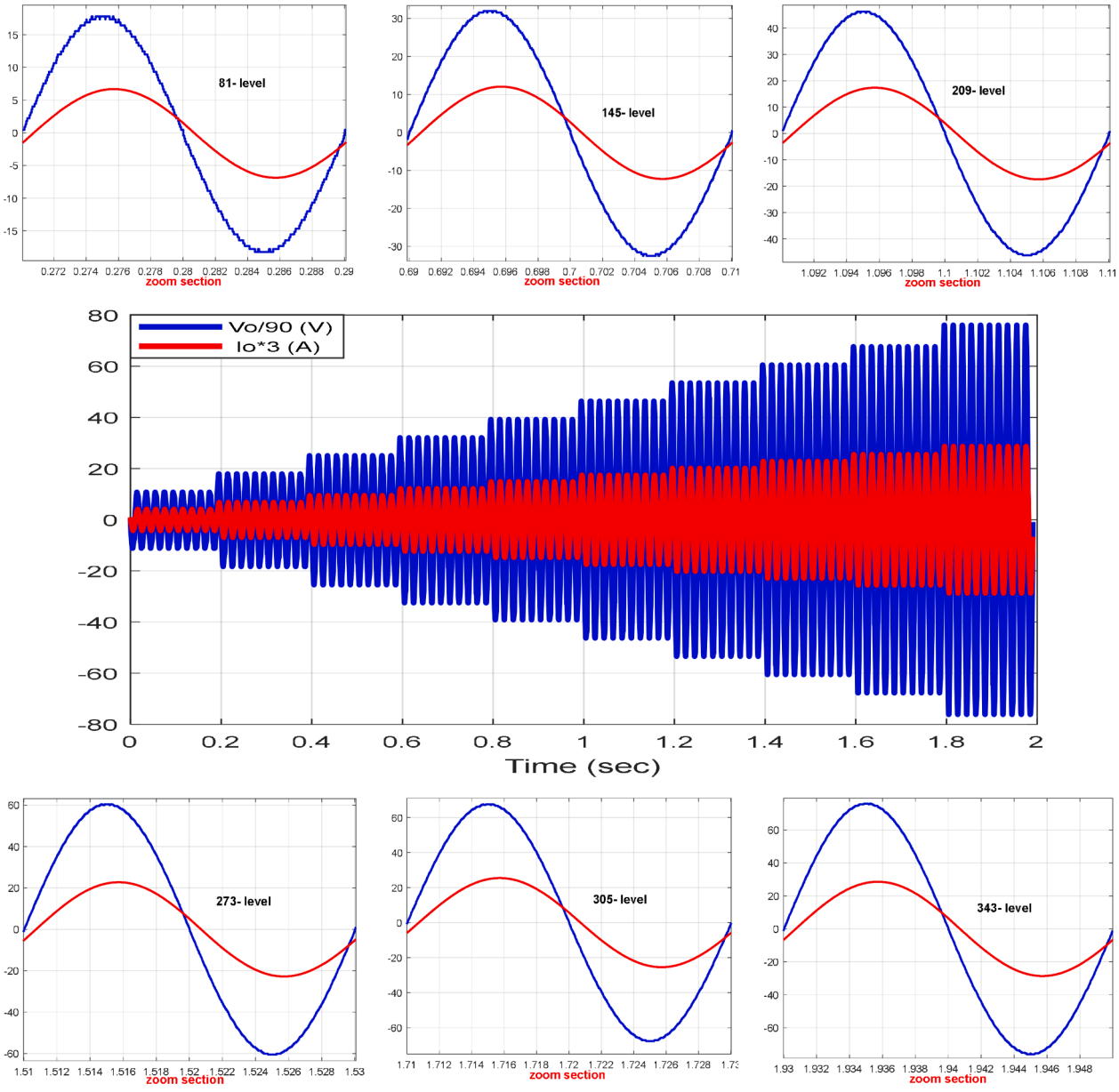


Fig. 18. System response at different levels.

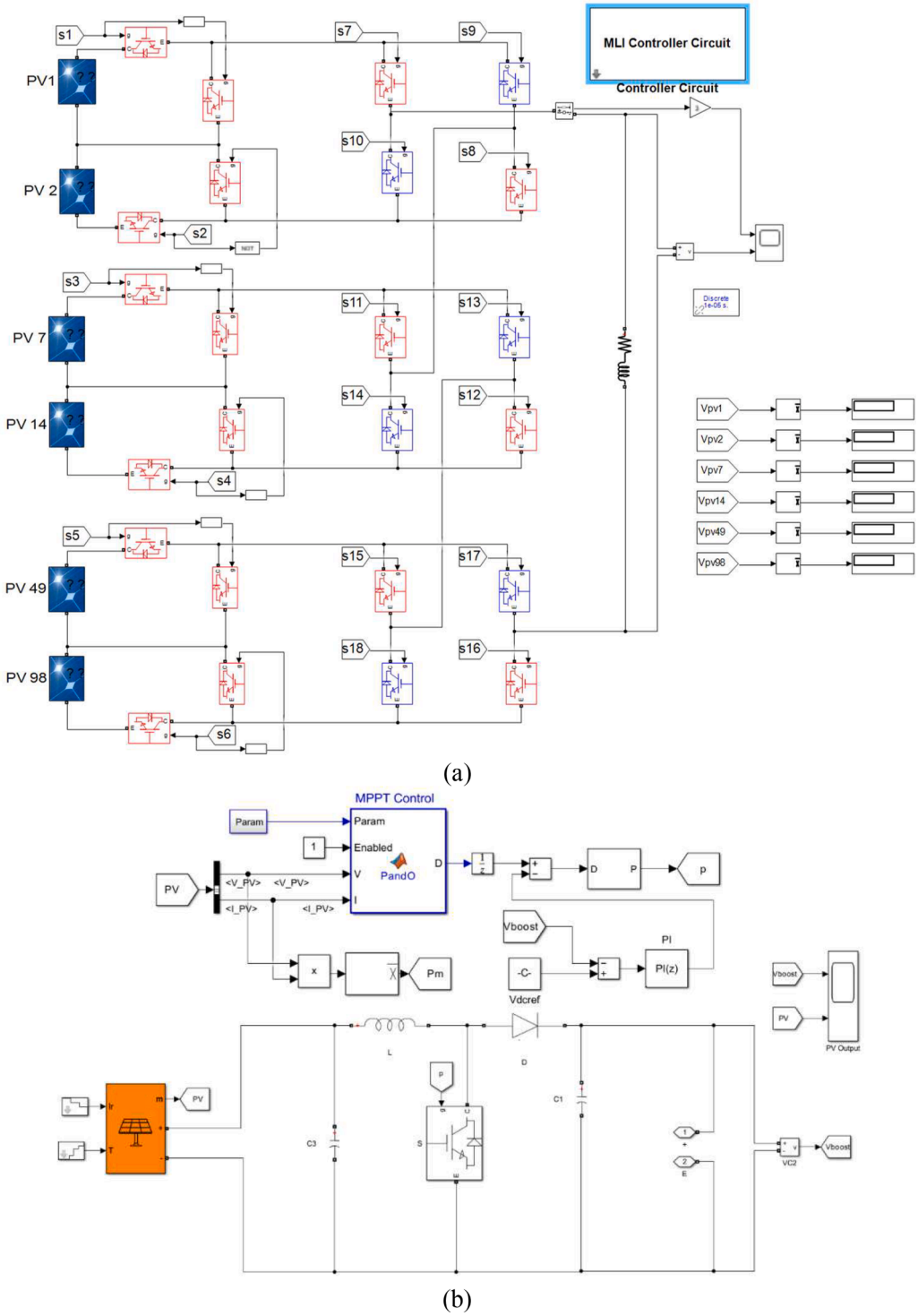


Fig. 19. Designed model of proposed 343-level inverter fed by PV sources.

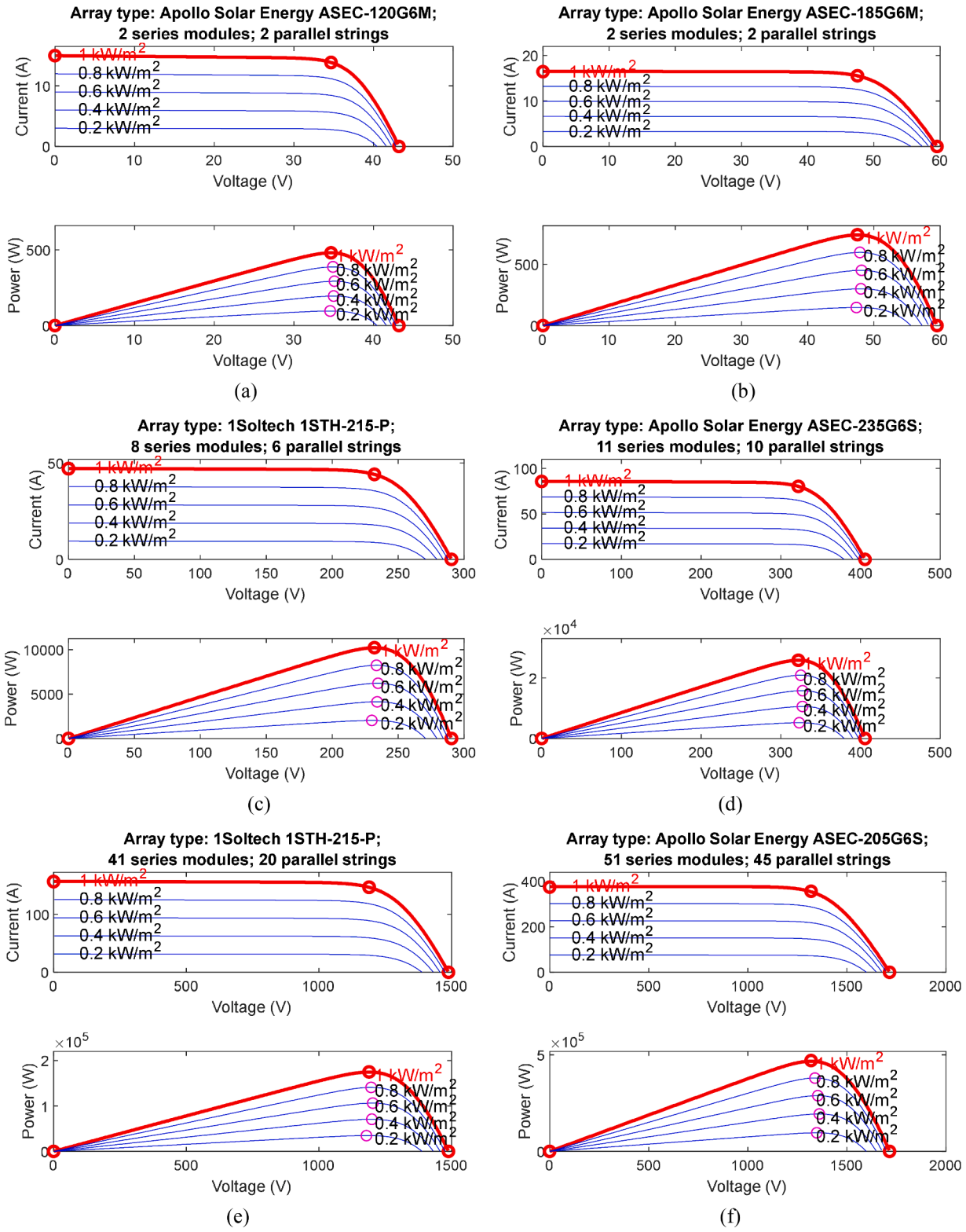


Fig. 20. The (V-I) and (P-V) characteristics of the (a) PV source 40 V, (b) PV source 80 V, (c) PV source 280 V, (d) PV source 560 V, (e) PV source 1960 V, and (f) PV source 3920 V.

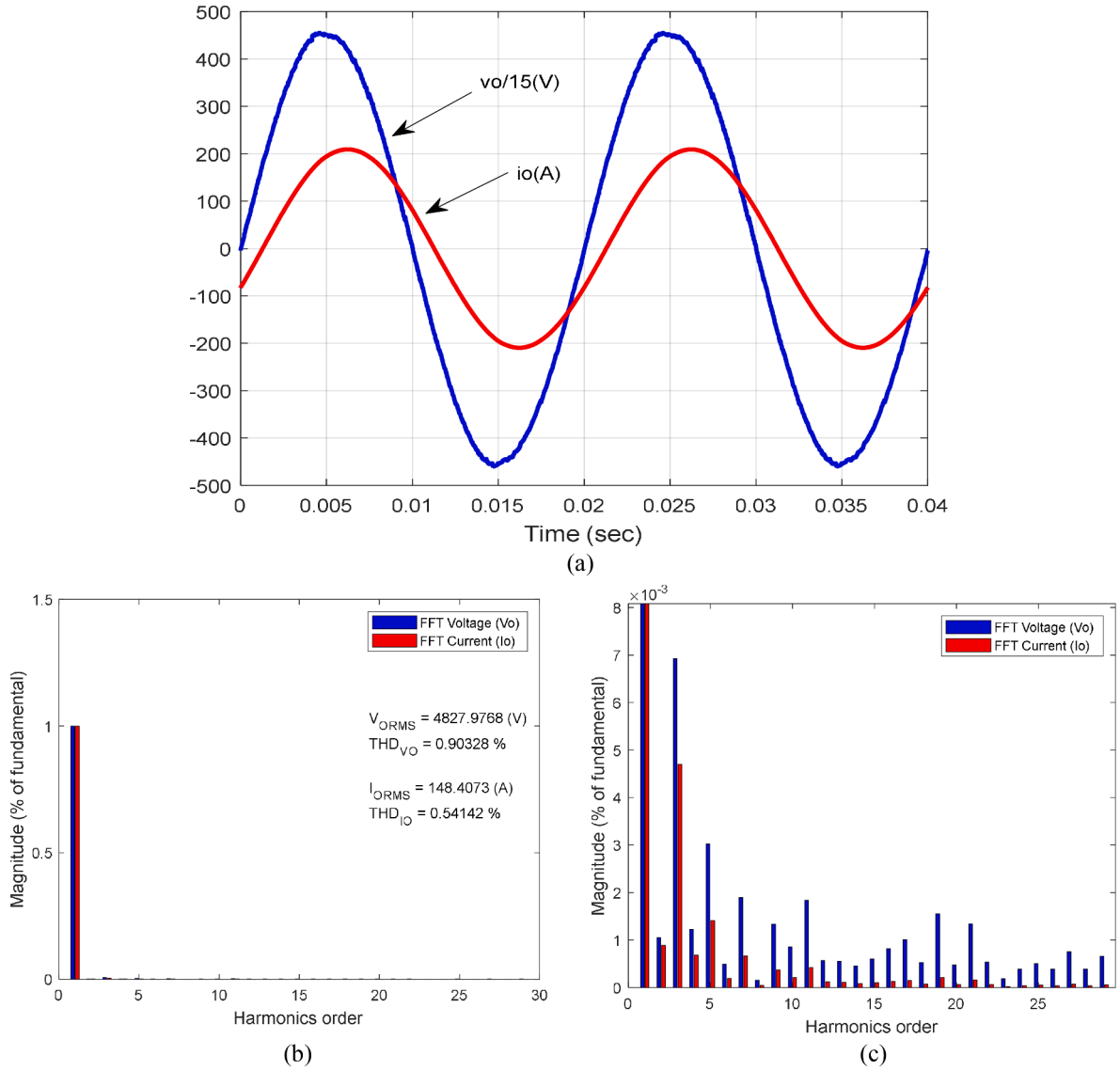


Fig. 21. 343-level simulation results: (a) output voltage and current, (b) FFT analyzer, and its (c) zoom section.

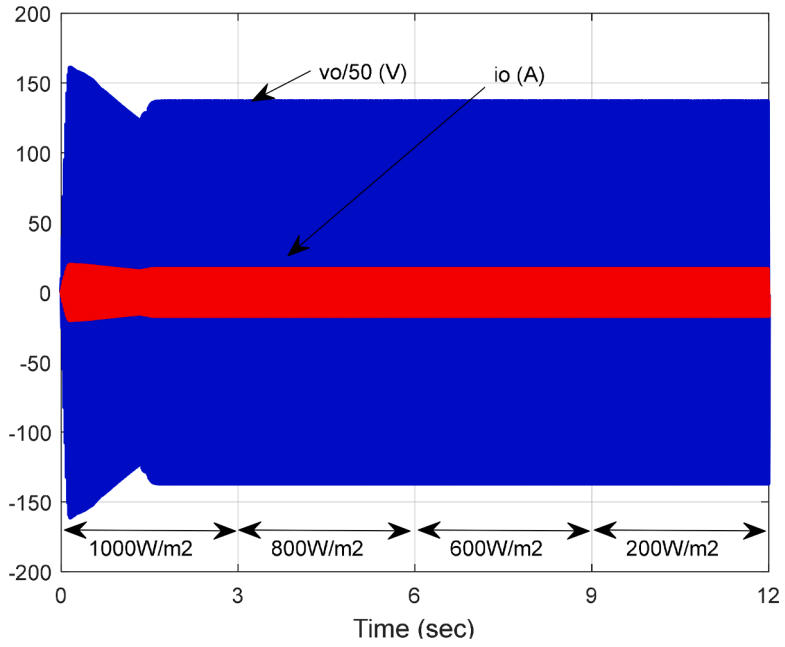


Fig. 22. Simulation results of the 343-level fed by PVs, output phase voltage and current with its variable irradiation at 25 °C with fixed output voltage.

level MLI designs. While References [35] and [38] achieve 125 levels using 20 switches, and Reference [37] achieves 81 levels with reduced switch count, the proposed configuration offers superior voltage resolution and THD performance. This validates the effectiveness of the asymmetric voltage ratio (1:2:7:14:49:98) in maximizing output levels while minimizing component requirements. Cost-Benefit Analysis: A comprehensive trade-off analysis reveals the economic advantages of the proposed topology. While the 18-switch configuration exceeds the component count of basic 2-level inverters (4 switches) or traditional 3-level NPC topologies (12 switches), the cost-effectiveness becomes evident when normalized per output voltage level. The proposed inverter achieves 19.06 levels per switch (343 levels ÷ 18 switches), significantly outperforming conventional configurations: a 3-level NPC achieves 0.25 levels/switch (3÷12), and even advanced 125-level designs achieve only 6.25 levels/switch (125÷20). Furthermore, the superior THD performance (0.32% vs. 2–4% for conventional topologies) eliminates the need for expensive passive filters, reducing overall system cost. The reduced voltage stress on individual switches (Vdc/2 max) enables use of lower-rated, less expensive semiconductor devices. When considering the total cost of ownership—including reduced filter requirements, lower switching losses at 3 kHz operation, and enhanced power quality—the proposed topology offers compelling economic benefits for high-performance renewable energy applications despite higher initial switch count. The whole simulation outcomes of the designed 343-level inverters with 18 switches reveal that from the power quality perspective, IEEE standard has been met.

5. Conclusion

The proposed asymmetrical 343-level cascaded inverter has shown enhanced solutions for power quality and harmonic distortion problems when interfaced with both DC sources and renewable energy systems. This study reveals that for three different operations, the inverter is able to produce low distortion, high quality sinusoidal waveforms. In all cases, the performances of the proposed power circuit and control strategy are demonstrated and confirmed, showing that the harmonics are well reduced, and the waveforms are clean. Nevertheless, the third case, which considers PV sources, has a slightly higher THD than the other two configurations; however, the obtained THD values are still low, which means that the inverter can be used in green energy standalone systems. The integration of DC and PV inputs makes the inverter suitable for a wide range of renewable energy applications. Furthermore, the modularity and cost-effectiveness of the system are demonstrated, as it employs only 18 switches to produce 343 voltage levels with low THD. It should be noted that the current study focuses on topology validation, voltage balancing capability, and output waveform quality through simulation-based analysis. Detailed efficiency estimation and comprehensive power loss analysis—including conduction losses, switching losses, and thermal modeling—were not included in this work. Based on preliminary calculations considering IGBT characteristics and switching frequency of 3 kHz, the estimated efficiency is expected to exceed 95% under rated conditions, though this requires experimental verification. These aspects will be thoroughly investigated in our upcoming experimental study, where we will evaluate practical efficiency based on device datasheets, measured waveforms, and thermal performance under various loading conditions. Topology Selection Rationale: This work specifically focuses on asymmetrical multilevel inverter topology rather than symmetrical configurations. The choice of asymmetrical design is deliberate and motivated by fundamental topological advantages: asymmetrical inverters achieve a very high number of levels with fewer switches, significantly reducing cost and complexity. For the proposed 343-level output, a symmetrical cascaded H-bridge inverter would require $2 \times (343–1) = 684$ switches (assuming H-bridge units), making it practically infeasible. Even optimized symmetrical designs would need substantially >18 switches. The asymmetric voltage ratio (1:2:7:14:49:98) enables maximum level generation with minimum component count, which is the core innovation of this work. Possible improvements for future studies include extending the study of the multi-level inverter design under different load conditions and incorporating more sophisticated control methods. Chosen asymmetrical inverter instead of symmetrical cause asymmetrical inverters achieve a very high number of levels with fewer switches, reducing cost and complexity. A symmetrical inverter would require significantly more devices to achieve 343 levels, making it less practical. Tests on real hardware should become part of future research to prove and verify the findings and strengthen the assertions. The research will execute real-world testing that enables evaluation of the system's performance within realistic operating environments. Experimental Validation: The current study establishes the theoretical foundation and simulation validation of the proposed 343-level inverter topology. We fully

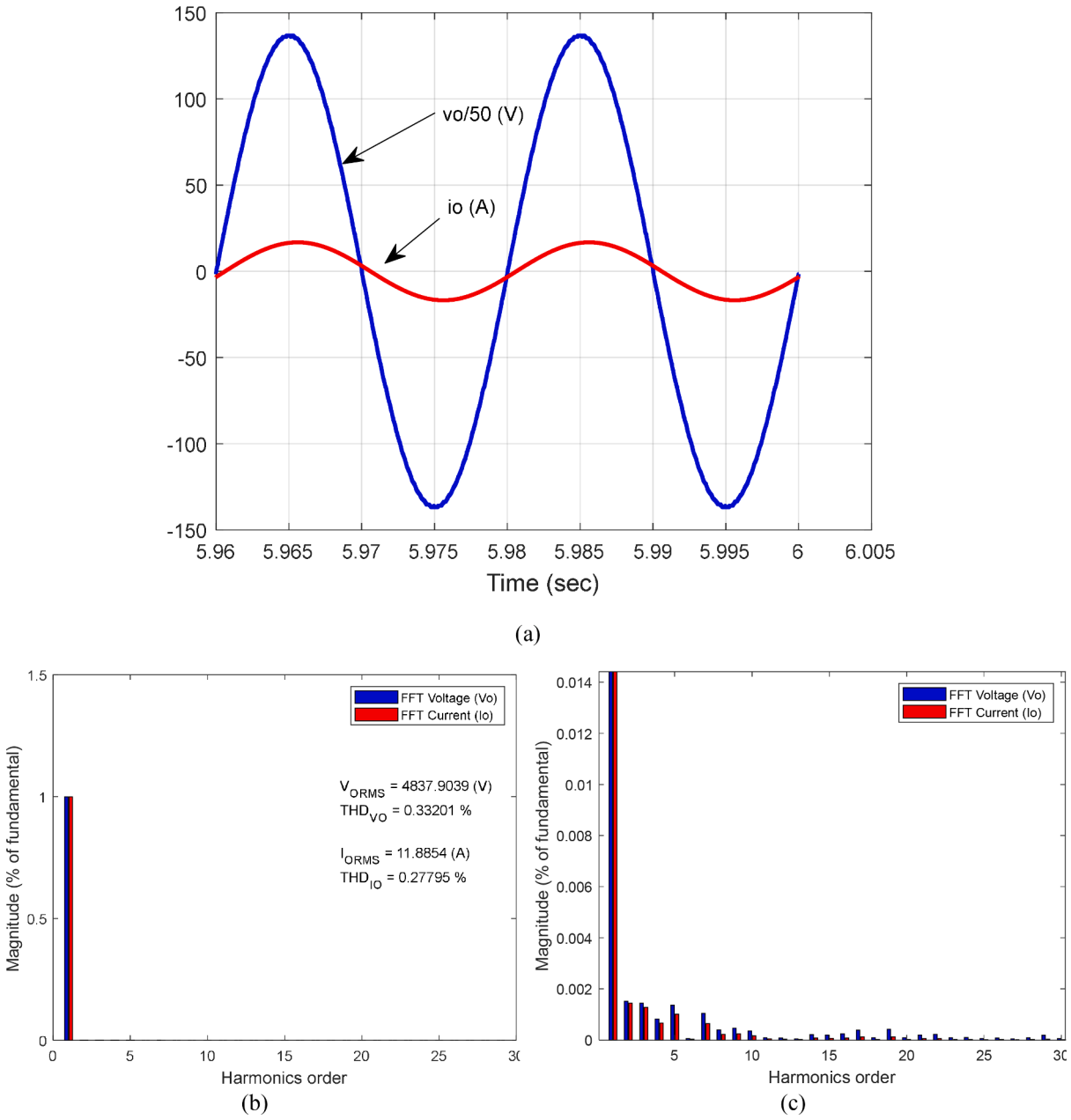


Fig. 23. Simulation results of the 343-level fed by PVs (a) output phase voltage and current with its (b) spectrum analyzer and (c) zoom section for the low harmonics order.

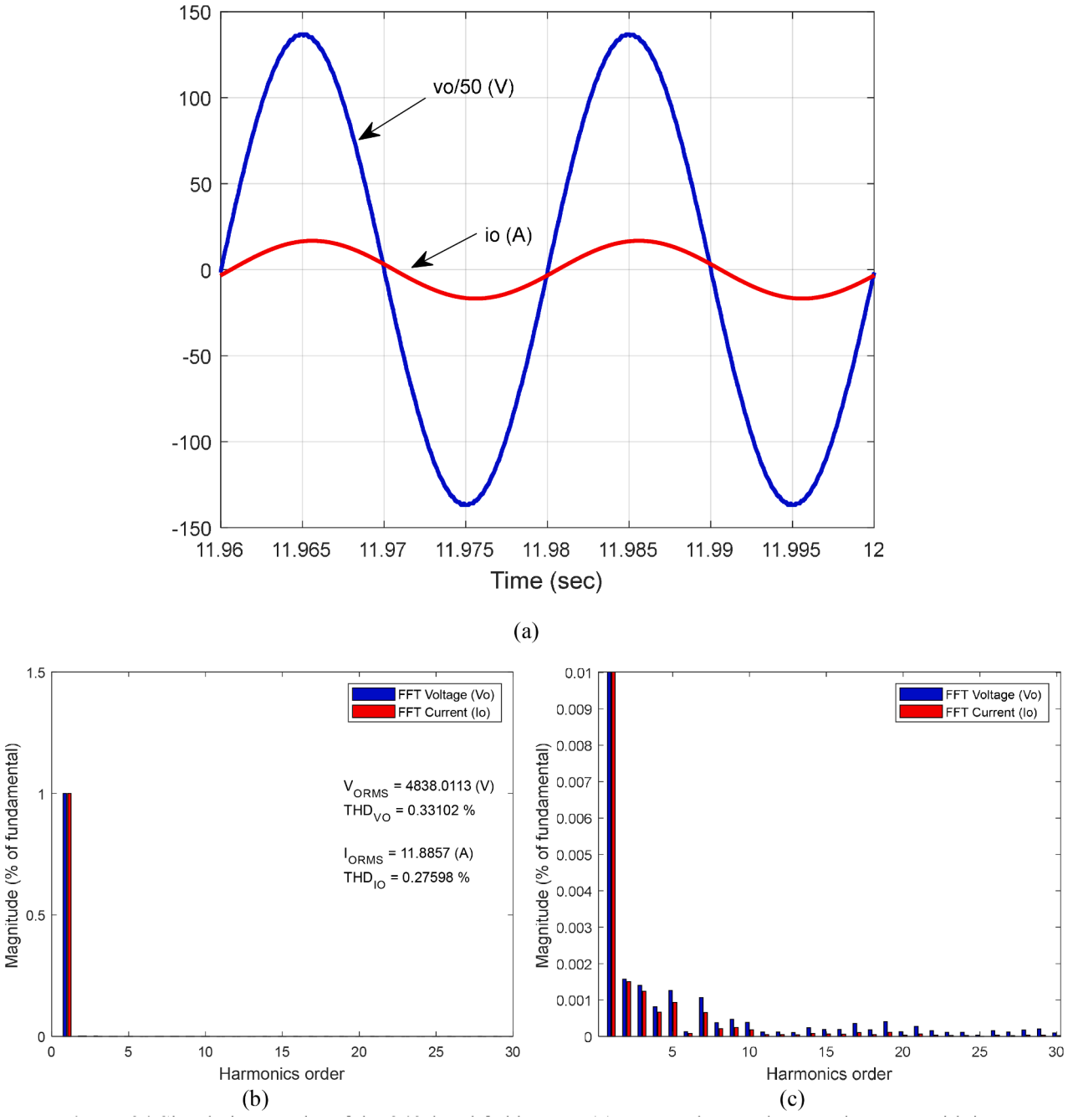


Fig. 24. Simulation results of the 343-level fed by PVs (a) output phase voltage and current with its (b) spectrum analyzer and (c) zoom section for the low harmonics order.

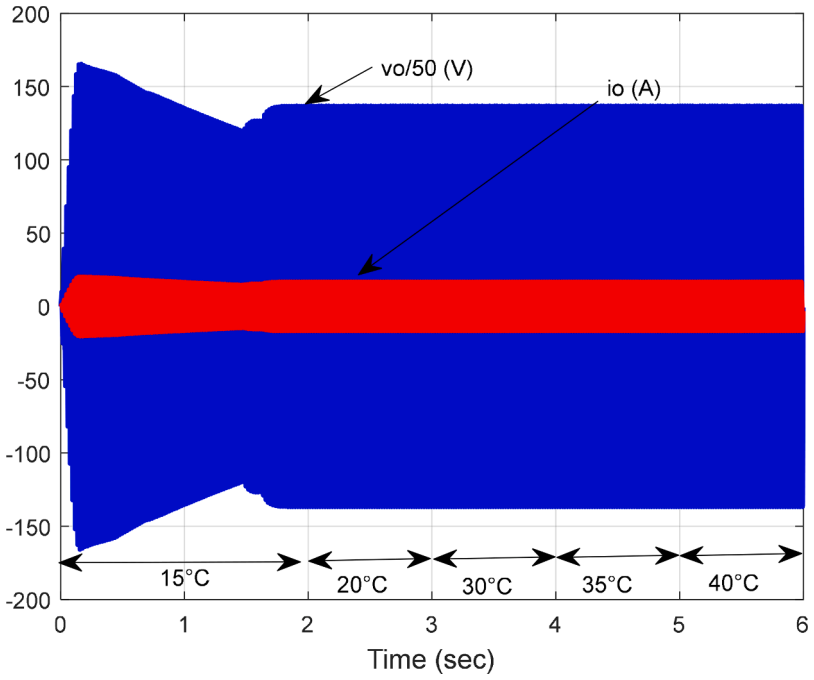


Fig. 25. Simulation results of the 343-level fed by PVs, output phase voltage and current with its 1000 W/m^2 irradiation at variable temperature with fixed output voltage.

acknowledge that hardware implementation and experimental validation are essential to confirm the practical viability of the design. Our planned future work includes: (1) development of a scaled laboratory prototype (1–5 kW) using commercial IGBT modules and DSP-based control; Hardware feasibility analysis indicates that the proposed topology is implementable using available semiconductor technology. For the 4.8 kV RMS output (6.8 kV peak), 6.5 kV/100A IGBT modules (e.g., Infineon FZ100R65KF1) or SiC MOSFETs (3.3 kV rated, series-connected) are suitable. Key implementation challenges include: (a) gate driver isolation—optical or magnetic isolation rated for 5 kV working voltage; (b) thermal management—estimated switching losses at 3 kHz are 150–200 W per switch, requiring forced air or liquid cooling; (c) voltage balancing resistors for series-connected devices; (d) PCB creepage/clearance distances >8 mm for 5 kV operation per IEC 60664; and (e) electromagnetic compatibility filtering for high dv/dt edges. These challenges are manageable with current technology and will be addressed in our experimental validation. (2) experimental verification of voltage balancing algorithms under dynamic conditions; (3) efficiency measurement and thermal performance evaluation; (4) grid-connection testing according to IEEE 1547 and IEC 61727 standards; and (5) long-term reliability assessment under varying environmental conditions. These experimental studies will validate the simulation results presented herein and provide practical insights into implementation challenges such as dead-time effects, device non-idealities, and electromagnetic compatibility considerations. Tests on real hardware should become part of future research to prove and verify the findings and strengthen the assertions. The research will execute real-world testing that enables evaluation of the system's performance within realistic operating conditions.

CRediT authorship contribution statement

Reving Masoud Abdulhakeem: Writing – original draft, Software, Methodology, Funding acquisition, Data curation. **Rakan Khalil Antar:** Validation, Supervision, Software, Resources, Conceptualization. **Ali Kircay:** Supervision, Project administration, Investigation. **Dilovan Asaad Zebari:** Writing – review & editing, Validation, Resources, Project administration.

Declaration of competing interest

The authors declare that they have no known conflict of interest regarding the publication of this article. This research was conducted independently without any financial support or commercial affiliation that could influence the results or interpretations of this study. The study presents the design, analysis, and simulation of an asymmetrical 343-level inverter for renewable energy applications, with a focus on its performance under varying energy sources such as battery and photovoltaic (PV) modules. The authors affirm that the findings are based solely on the results of the simulations conducted and that no external parties have had any role in the study's design or interpretation.

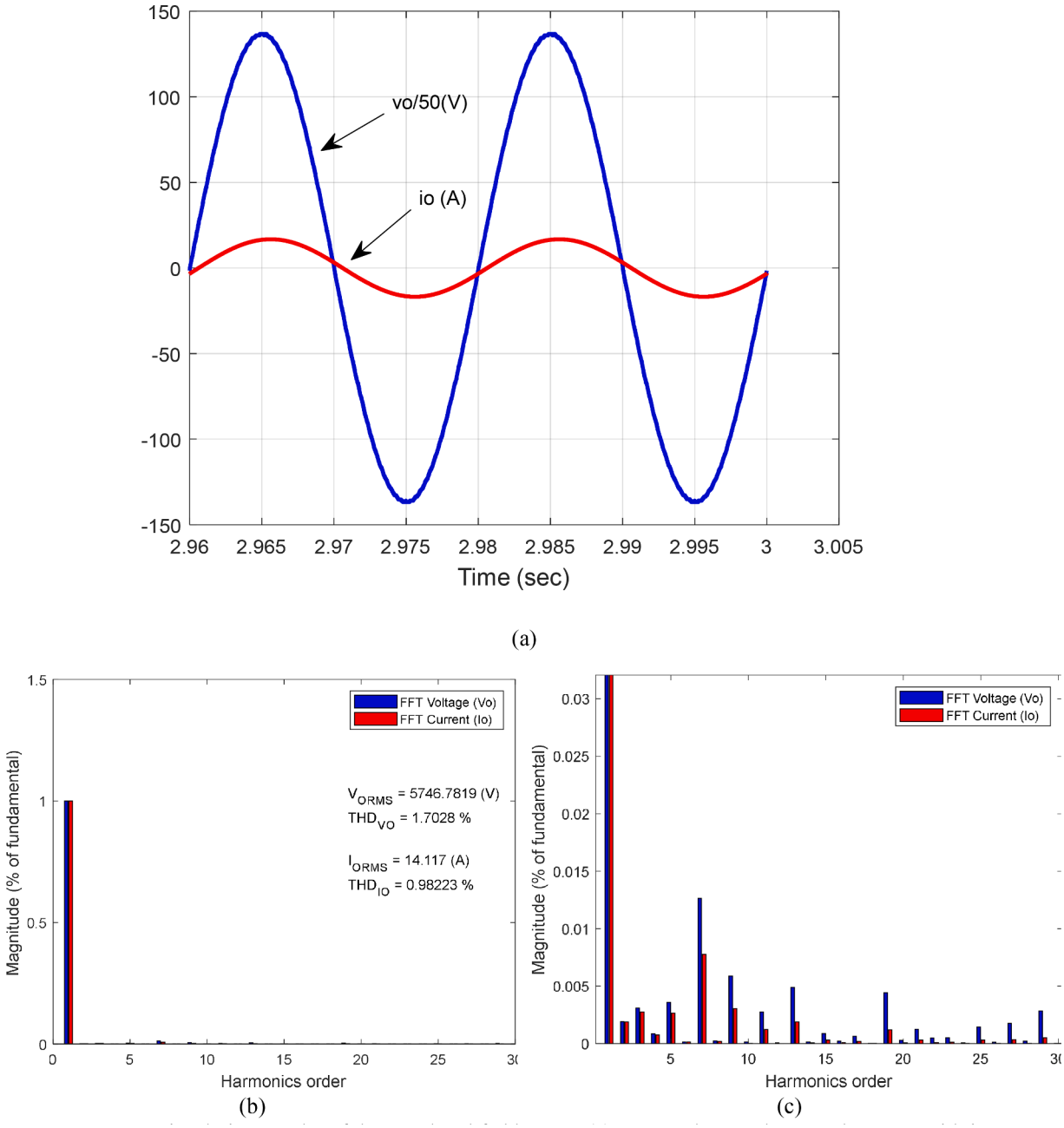


Fig. 26. Simulation results of the 343-level fed by PVs (a) output phase voltage and current with its (b) spectrum analyzer and (c) zoom section for the low harmonics order.

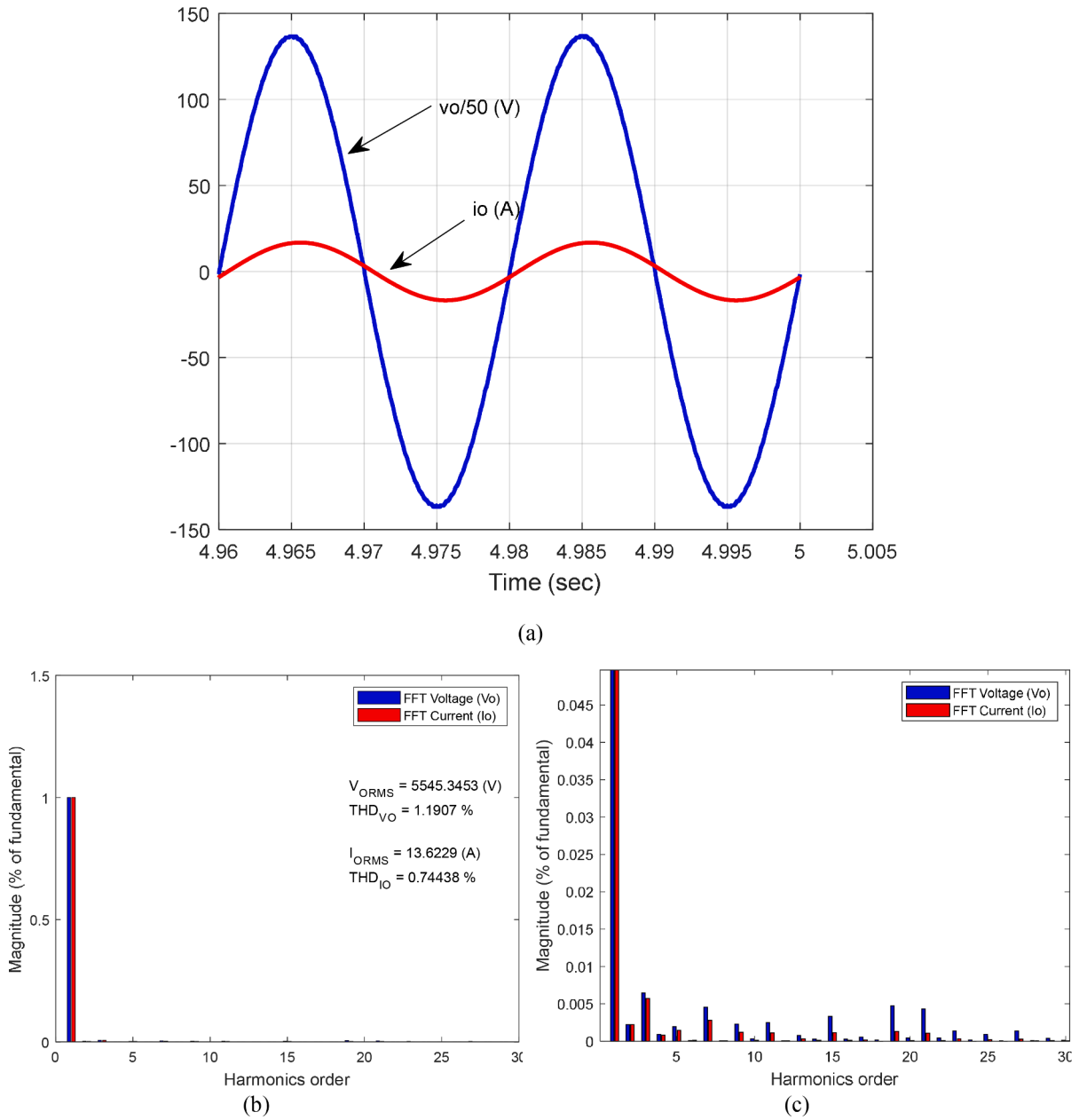


Fig. 27. Simulation results of the 343-level fed by PVs (a) output phase voltage and current with its (b) spectrum analyzer and (c) zoom section for the low harmonics order.

Table 4
Review of 343-level and related MLI designs.

Ref.	Levels	No. of Switches	No. of Diodes	Input Sources	THD_{Vo}	THD_{Io}
[23]	7	14	-	Solar PV	3.4%	2.1%
[33]	Varies (Multiple)	Varies (Multiple)	-	Solar PV + Wind	4.1%	2.2%
[35]	125	20	–	DC source	~1.2%	~0.9%
[36]	≥127 (reviewed designs)	Varies (reduced)	–	DC/PV	<2% (reported)	<2% (reported)
[37]	81	Reduced	-	DC source	~1.5%	~1.2%
[38]	125	20	-	DC source	~1.2%	~0.9%
Proposed Circuit	343	18	-	DC Battery (1:2:7:14:49:98)V per unit system	0.32422%	0.32422%
Proposed Circuit	343	18	-	DC Battery (40:80:280:560:1960:3920) Actual voltage system	0.32414%	0.25682%
Proposed Circuit	343	18	-	PVs System(40:80:280:560: 1960:3920)V	0.90328%	0.54142%

Table 5
Summary of performance metrics across all operating configurations.

Parameter	Case 1: Per-Unit (1Vdc)	Case 2: Actual (40Vdc)	Case 3: PV-Based
Input Configuration	(1:2:7:14:49:98)V	(40:80:280:560:1960:3920)V	PV arrays with boost converters that produce same voltages as in case 2
Power Factor	0.92	0.97	0.92
Load (R, L)	30 Ω, 40 mH	700 Ω, 500 mH	700 Ω, 500 mH
Vo,RMS	120.93 V	4838.76 V	4827.98 V
Io,RMS	3.72 A	6.74 A	148.41 A
THDVo (343-level)	0.324%	0.324%	0.903%
THDIo (343-level)	0.225%	0.257%	0.541%
Switching Frequency	3 kHz	3 kHz	3 kHz
Apparent Power (S)	1348.8 VA	97.9 kVA	716.5 kVA
Real Power (P)	1243.9 W	95.5 kW	659.2 kW

Appendix

Switching state patterns of 343 level

Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18
0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	1	1	0	0	1	0	1	0	1	0	1	0
2	0	1	0	0	0	0	1	1	0	0	1	0	1	0	1	0	1	0
3	1	1	0	0	0	0	1	1	0	0	1	0	1	0	1	0	1	0
4	1	1	1	0	0	0	0	0	1	1	1	1	0	0	1	0	1	0
5	0	1	1	0	0	0	0	0	1	1	1	1	0	0	1	0	1	0
6	1	0	1	0	0	0	0	0	1	1	1	1	0	0	1	0	1	0
7	0	0	1	0	0	0	1	0	1	0	1	1	0	0	1	0	1	0
8	1	0	1	0	0	0	1	1	0	0	1	1	0	0	1	0	1	0
9	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	0	1	0
10	1	1	1	0	0	0	1	1	0	0	1	1	0	0	1	0	1	0
11	1	1	0	1	0	0	0	0	1	1	1	1	0	0	1	0	1	0
12	0	1	0	1	0	0	0	0	1	1	1	1	0	0	1	0	1	0
13	1	0	0	1	0	0	0	0	1	1	1	1	0	0	1	0	1	0
14	0	0	0	1	0	0	1	0	1	0	1	1	0	0	1	0	1	0
15	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	0	1	0
16	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	0	1	0
17	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1	0	1	0
18	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0	1	0
19	0	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0	1	0
20	1	0	1	1	0	0	0	0	1	1	1	1	0	0	1	0	1	0
21	0	0	1	1	0	0	1	0	1	0	1	1	0	0	1	0	1	0
22	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	0	1	0
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24	1	1	1	1	0	0	1	1	0	0	1	1	0	0	1	0	1	0
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52	1	1	0	0	1	0	1	1	0	0	1	0	1	0	1	1	0	0
53	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	0	0

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Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18
54	0	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	0	0
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56	0	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0	0
57	1	0	1	0	1	0	1	1	0	0	1	1	0	0	1	1	0	0
58	0	1	1	0	1	0	1	1	0	0	1	1	0	0	1	1	0	0
59	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	1	0	0
60	1	1	0	1	1	0	0	0	1	1	1	1	0	0	1	1	0	0
61	0	1	0	1	1	0	0	0	1	1	1	1	0	0	1	1	0	0
62	1	0	0	1	1	0	0	0	1	1	1	1	0	0	1	1	0	0
63	0	0	0	1	1	0	1	0	1	0	1	1	0	0	1	1	0	0
64	1	0	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0
65	0	1	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0
66	1	1	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0
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68	0	1	1	1	1	0	0	0	1	1	1	1	0	0	1	1	0	0
69	1	0	1	1	1	0	0	0	1	1	1	1	0	0	1	1	0	0
70	0	0	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	0
71	1	0	1	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0
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98	0	0	0	0	0	1	1	0	1	0	1	0	1	0	1	1	0	0
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100	0	1	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0
101	1	1	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0
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107	0	1	1	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0
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125	1	0	1	1	1	1	0	0	1	1	0	0	1	1	1	1	0	0
126	0	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0
127	1	0	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0
128	0	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0
129	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0

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Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18
130	1	1	0	1	1	1	0	0	1	1	0	0	1	1	1	1	0	0
131	0	1	0	1	1	1	0	0	1	1	0	0	1	1	1	1	0	0
132	1	0	0	1	1	1	0	0	1	1	0	0	1	1	1	1	0	0
133	0	0	0	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0
134	1	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0
135	0	1	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0
136	1	1	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0
137	1	1	1	0	1	1	0	0	1	1	0	0	1	1	1	1	0	0
138	0	1	1	0	1	1	0	0	1	1	0	0	1	1	1	1	0	0
139	1	0	1	0	1	1	0	0	1	1	0	0	1	1	1	1	0	0
140	0	0	1	0	1	1	1	0	1	0	0	0	1	1	1	1	0	0
141	1	0	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
142	0	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
143	1	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
144	1	1	0	0	1	1	0	0	1	1	1	0	1	0	1	1	0	0
145	0	1	0	0	1	1	0	0	1	1	1	0	1	0	1	1	0	0
146	1	0	0	0	1	1	0	0	1	1	1	0	1	0	1	1	0	0
147	0	0	0	0	1	1	1	0	1	0	1	0	1	0	1	1	0	0
148	1	0	0	0	1	1	1	1	0	0	1	0	1	0	1	1	0	0
149	0	1	0	0	1	1	1	1	0	0	1	0	1	0	1	1	0	0
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151	1	1	1	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0
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153	1	0	1	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0
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158	1	1	0	1	1	1	0	0	1	1	1	1	0	0	1	1	0	0
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166	0	1	1	1	1	1	0	0	1	1	1	1	0	0	1	1	0	0
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168	0	0	1	1	1	1	1	0	1	0	1	1	0	0	1	1	0	0
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171	1	1	1	1	1	1	1	1	0	0	1	1	0	0	1	1	0	0
−1	1	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1	0
−2	0	1	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1	0
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−4	1	1	1	0	0	0	1	1	0	0	0	0	1	1	1	0	1	0
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−10	1	1	1	0	0	0	0	0	1	1	0	0	1	1	1	0	1	0
−11	1	1	0	1	0	0	1	1	0	0	0	0	1	1	1	0	1	0
−12	0	1	0	1	0	0	1	1	0	0	0	0	1	1	1	0	1	0
−13	1	0	0	1	0	0	1	1	0	0	0	0	1	1	1	0	1	0
−14	0	0	0	1	0	0	1	0	1	0	0	0	1	1	1	0	1	0
−15	1	0	0	1	0	0	0	0	1	1	0	0	1	1	1	0	1	0
−16	0	1	0	1	0	0	0	0	1	1	0	0	1	1	1	0	1	0
−17	1	1	0	1	0	0	0	0	1	1	0	0	1	1	1	0	1	0
−18	1	1	1	1	0	0	1	1	0	0	0	0	1	1	1	0	1	0
−19	0	1	1	1	0	0	1	1	0	0	0	0	1	1	1	0	1	0
−20	1	0	1	1	0	0	1	1	0	0	0	0	1	1	1	0	1	0
−21	0	0	1	1	0	0	1	0	1	0	0	0	1	1	1	0	1	0
−22	1	0	1	1	0	0	0	0	1	1	0	0	1	1	1	0	1	0
−23	0	1	1	1	0	0	0	0	1	1	0	0	1	1	1	0	1	0
−24	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	0	1	0
−25	1	1	1	1	1	0	1	1	0	0	1	1	0	0	0	0	1	1
−26	0	1	1	1	1	0	1	1	0	0	1	1	0	0	0	0	1	1
−27	1	0	1	1	1	0	1	1	0	0	1	1	0	0	0	0	1	1
−28	0	0	1	1	1	0	1	0	1	0	1	1	0	0	0	0	1	1
−29	1	0	1	1	1	0	0	0	1	1	1	1	0	0	0	0	1	1
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−31	1	1	1	1	1	0	0	0	1	1	1	1	0	0	0	0	1	1
−32	1	1	0	1	1	0	1	1	0	0	1	1	0	0	0	0	1	1
−33	0	1	0	1	1	0	1	1	0	0	1	1	0	0	0	0	1	1
−34	1	0	0	1	1	0	1	1	0	0	1	1	0	0	0	0	1	1

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Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18
−35	0	0	0	1	1	0	1	0	1	0	1	1	0	0	0	0	1	1
−36	1	0	0	1	1	0	0	0	1	1	1	1	0	0	0	0	1	1
−37	0	1	0	1	1	0	0	0	1	1	1	1	0	0	0	0	1	1
−38	1	1	0	1	1	0	0	0	1	1	1	1	0	0	0	0	1	1
−39	1	1	1	0	1	0	1	1	0	0	1	1	0	0	0	0	1	1
−40	0	1	1	0	1	0	1	1	0	0	1	1	0	0	0	0	1	1
−41	1	0	1	0	1	0	1	1	0	0	1	1	0	0	0	0	1	1
−42	0	0	1	0	1	0	1	0	1	0	1	1	0	0	0	0	1	1
−43	1	0	1	0	1	0	0	0	1	1	1	1	0	0	0	0	1	1
−44	0	1	1	0	1	0	0	0	1	1	1	1	0	0	0	0	1	1
−45	1	1	1	0	1	0	0	0	1	1	1	1	0	0	0	0	1	1
−46	1	1	0	0	1	0	1	1	0	0	1	0	1	0	0	0	1	1
−47	0	1	0	0	1	0	1	1	0	0	1	0	1	0	0	0	1	1
−48	1	0	0	0	1	0	1	1	0	0	1	0	1	0	0	0	1	1
−49	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	1	1
−50	1	0	0	0	1	0	0	0	1	1	1	0	1	0	0	0	1	1
−51	0	1	0	0	1	0	0	0	1	1	1	0	1	0	0	0	1	1
−52	1	1	0	0	1	0	0	0	1	1	1	0	1	0	0	0	1	1
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−55	1	0	1	0	1	0	1	1	0	0	0	0	1	1	0	0	1	1
−56	0	0	1	0	1	0	1	0	1	0	0	0	1	1	0	0	1	1
−57	1	0	1	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1
−58	0	1	1	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1
−59	1	1	1	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1
−60	1	1	0	1	1	0	1	1	0	0	0	0	1	1	0	0	1	1
−61	0	1	0	1	1	0	1	1	0	0	0	0	1	1	0	0	1	1
−62	1	0	0	1	1	0	1	1	0	0	0	0	1	1	0	0	1	1
−63	0	0	0	1	1	0	1	0	1	0	0	0	1	1	0	0	1	1
−64	1	0	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1
−65	0	1	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1
−66	1	1	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1
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−68	0	1	1	1	1	0	1	1	0	0	0	0	1	1	0	0	1	1
−69	1	0	1	1	1	0	1	1	0	0	0	0	1	1	0	0	1	1
−70	0	0	1	1	1	0	1	0	1	0	0	0	1	1	0	0	1	1
−71	1	0	1	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1
−72	0	1	1	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1
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−90	1	0	1	0	0	1	1	1	0	0	1	1	0	0	0	0	1	1
−91	0	0	1	0	0	1	1	0	1	0	1	1	0	0	0	0	1	1
−92	1	0	1	0	0	1	0	0	1	1	1	1	0	0	0	0	1	1
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−96	0	1	0	0	0	1	1	1	0	0	1	0	1	0	0	0	1	1
−97	1	0	0	0	0	1	1	1	0	0	1	0	1	0	0	0	1	1
−98	0	0	0	0	0	1	1	0	1	0	1	0	1	0	0	0	1	1
−99	1	0	0	0	0	1	0	0	1	1	1	0	1	0	0	0	1	1
−100	0	1	0	0	0	1	0	0	1	1	1	0	1	0	0	0	1	1
−101	1	1	0	0	0	1	0	0	1	1	1	0	1	0	0	0	1	1
−102	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	1	1
−103	0	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	1	1
−104	1	0	1	0	0	1	1	1	0	0	0	0	1	1	0	0	1	1
−105	0	0	1	0	0	1	1	0	1	0	0	0	1	1	0	0	1	1
−106	1	0	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1
−107	0	1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1
−108	1	1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1
−109	1	1	0	1	0	1	1	1	0	0	0	0	1	1	0	0	1	1
−110	0	1	0	1	0	1	1	1	0	0	0	0	1	1	0	0	1	1

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Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18
−111	1	0	0	1	0	1	1	1	0	0	0	0	1	1	0	0	1	1
−112	0	0	0	1	0	1	1	0	1	0	0	0	1	1	0	0	1	1
−113	1	0	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
−114	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
−115	1	1	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
−116	1	1	1	1	0	1	1	1	0	0	0	0	1	1	0	0	1	1
−117	0	1	1	1	0	1	1	1	0	0	0	0	1	1	0	0	1	1
−118	1	0	1	1	0	1	1	1	0	0	0	0	1	1	0	0	1	1
−119	0	0	1	1	0	1	1	0	1	0	0	0	1	1	0	0	1	1
−120	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
−121	0	1	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
−122	1	1	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
−123	1	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	1	1
−124	0	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	1	1
−125	1	0	1	1	1	1	1	1	0	0	1	1	0	0	0	0	1	1
−126	0	0	1	1	1	1	1	0	1	0	1	1	0	0	0	0	1	1
−127	1	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
−128	0	1	1	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
−129	1	1	1	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
−130	1	1	0	1	1	1	1	1	0	0	1	1	0	0	0	0	1	1
−131	0	1	0	1	1	1	1	1	0	0	1	1	0	0	0	0	1	1
−132	1	0	0	1	1	1	1	1	0	0	1	1	0	0	0	0	1	1
−133	0	0	0	1	1	1	1	0	1	0	1	1	0	0	0	0	1	1
−134	1	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
−135	0	1	0	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
−136	1	1	0	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
−137	1	1	1	0	1	1	1	1	0	0	1	1	0	0	0	0	1	1
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−139	1	0	1	0	1	1	1	1	0	0	1	1	0	0	0	0	1	1
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−141	1	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
−142	0	1	1	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
−143	1	1	1	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
−144	1	1	0	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1
−145	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1
−146	1	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1
−147	0	0	0	0	1	1	1	0	1	0	1	0	1	0	0	0	1	1
−148	1	0	0	0	1	1	0	0	1	1	1	0	1	0	0	0	1	1
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−151	1	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1
−152	0	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1
−153	1	0	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1
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−157	1	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
−158	1	1	0	1	1	1	1	1	0	0	0	0	1	1	0	0	1	1
−159	0	1	0	1	1	1	1	1	0	0	0	0	1	1	0	0	1	1
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−161	0	0	0	1	1	1	1	0	1	0	0	0	1	1	0	0	1	1
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−163	0	1	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1
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−169	1	0	1	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1
−170	0	1	1	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1
−171	1	1	1	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Data availability

Data will be made available on request.

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